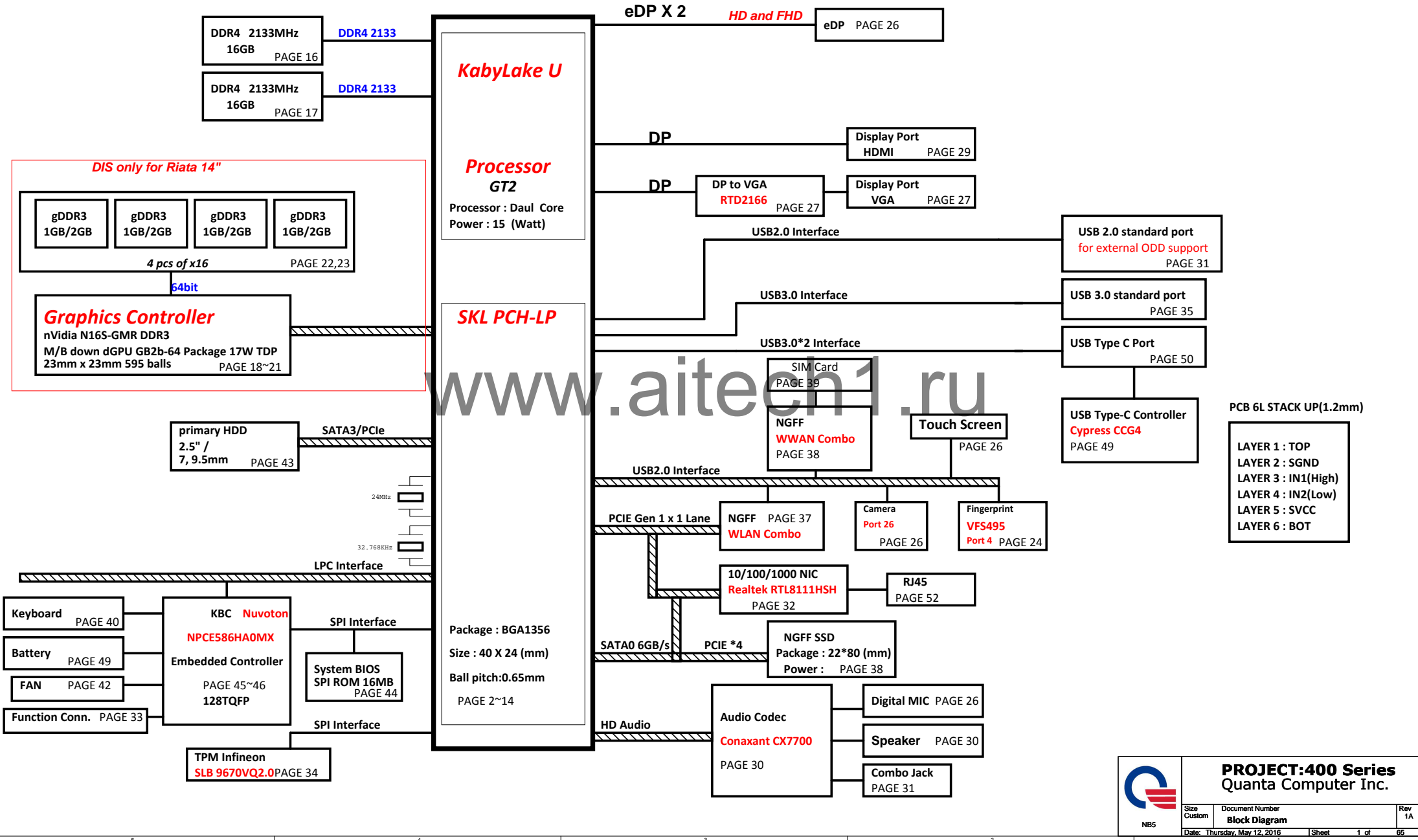
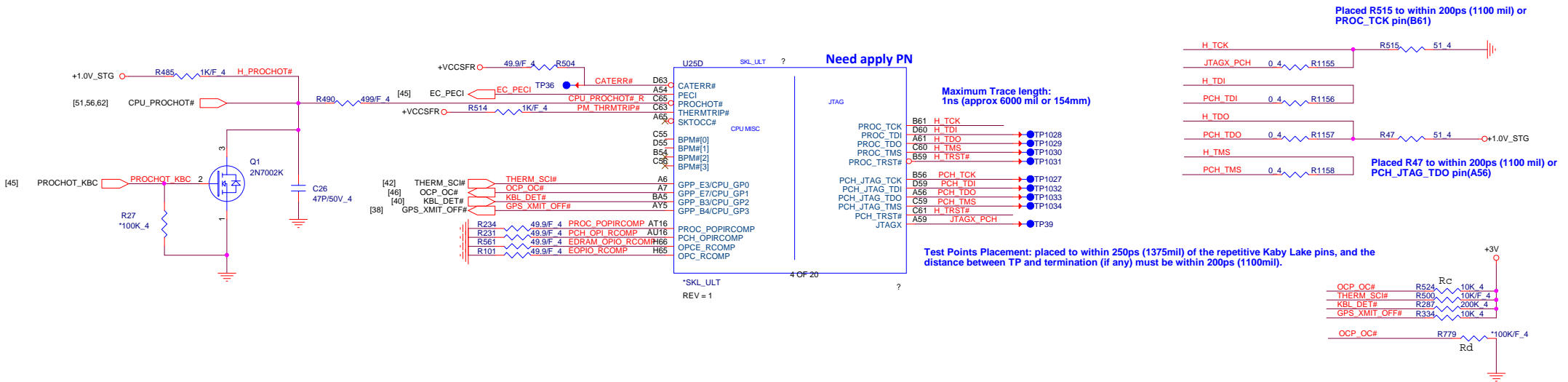
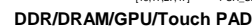
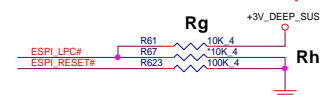


# Reilly 13"/Rourke 14" KabyLake -U (UMA/DIS) Schematics01

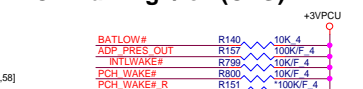
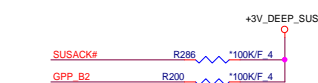




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### PCH Pull-high/low(CLG)

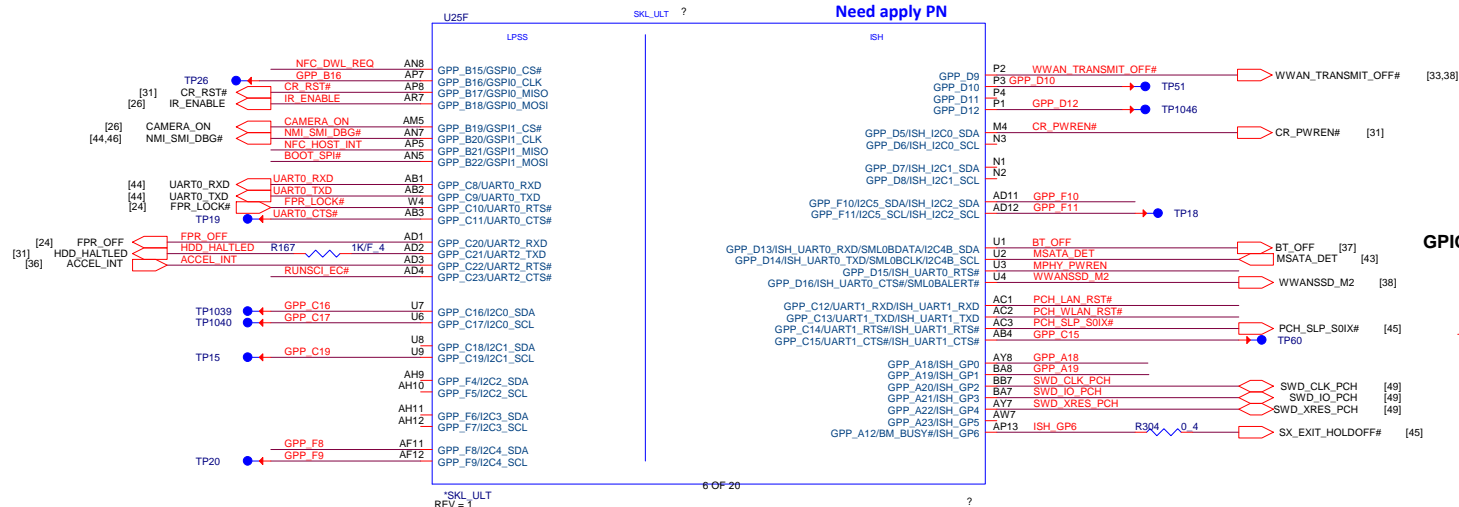


For DS3      -->Ra  
Non-DS3    -->Rb

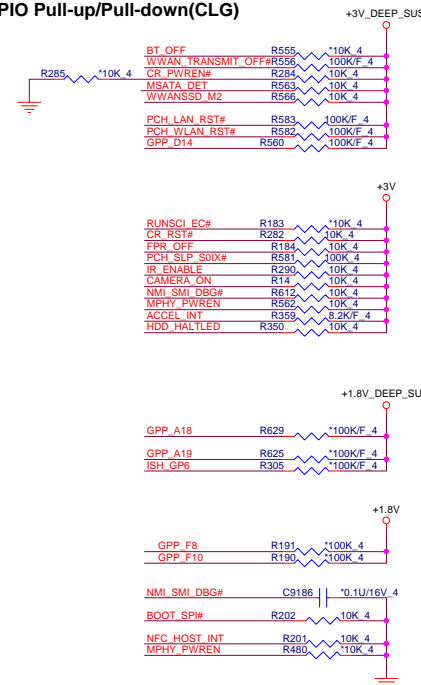
Ra



Size Custom	Document Number <b>03 – SKYLAKE (SPI/LPC/SMB/PM)</b>	Rev 1A
Date: Thursday, May 12, 2016	Sheet 3 of	65



### GPIO Pull-up/Pull-down(CLG)



Codec table

	CX7700	CX7501
R206	INSTAL	UNINSTAL
R207	UNINSTAL	INSTAL

[2,3,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63]

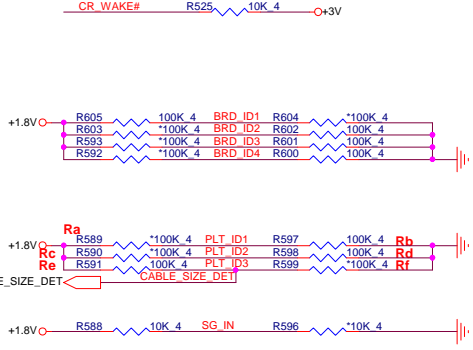
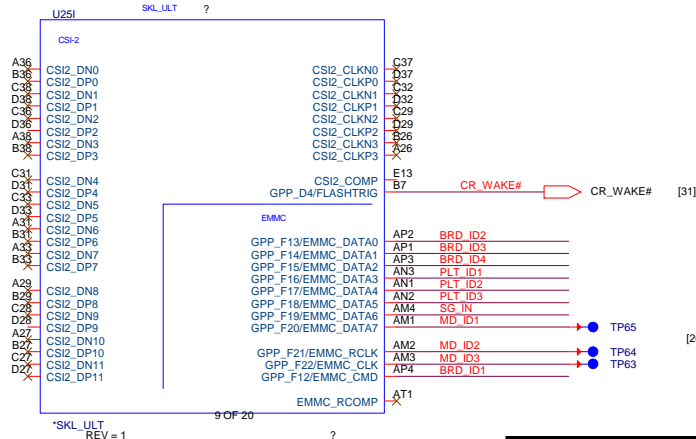


**PROJECT:400 Series**  
Quanta Computer Inc.

Size Custom	Document Number <b>04 – SKYLAKE (GPIO)</b>	Rev 1/
Date: Thursday, May 12, 2016	Sheet	4 of 65



	BRD_ID1	BRD_ID2	BRD_ID3	BRD_ID4	AMD_FCH
	GPIO201	GPIO202	GPIO203	GPIO204	PPMT
	GPIO14	GPIO34	GPIO35	GPIO40	LPI-H
BOARD REVISION	GPIO15	GPIO34	GPIO35	GPIO40	LPI-H
	GPIO76	GPIO77	GPIO78	GPIO79	LPT-LP
DB0	0	0	0	0	
DB1	0	0	0	1	
DB2	0	0	1	0	
	0	0	1	1	
SI1	0	1	0	0	
SIB	0	1	0	1	
SI2	0	1	1	0	
	0	1	1	1	
Pre-PV	1	0	0	0	
PV	1	0	0	1	
	1	0	1	0	
	1	0	1	1	
MV1	1	1	0	0	
	1	1	0	1	
	1	1	1	0	
	1	1	1	1	



PLT_ID1	PLT_ID2	PLT_ID3	
Ra	Rc	Re	H
Rb	Rd	Rf	L
0	0	0	13.3"
0	0	1	14"
0	1	0	15.6"
0	1	1	17.3"

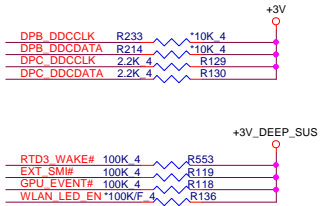
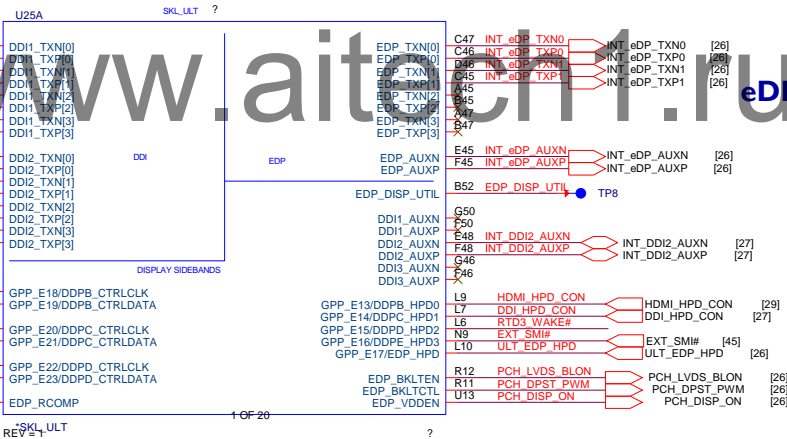
SG_IN	
DIS=1	R588 (Default)
UMA=0	R596

UNINSTAL

HDMI

VGA

eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



PROJECT:400 Series  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	05 - SKYLAKE (eDP/DDI/Board ID)	1A
Date: Thursday, May 12, 2016	Sheet	5 of 65

## SkyLake ULT Processor (DDR4)

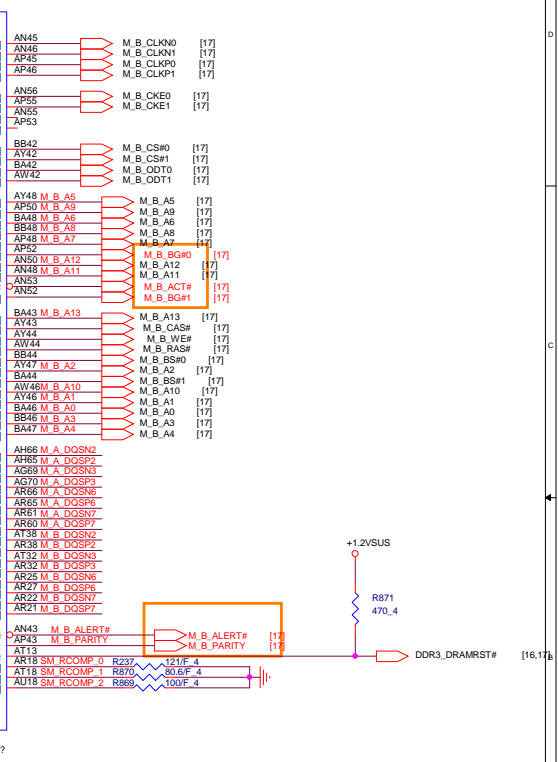
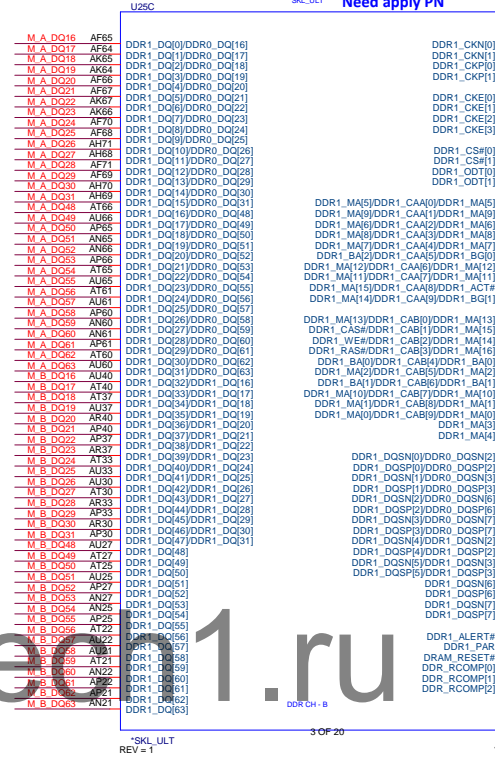
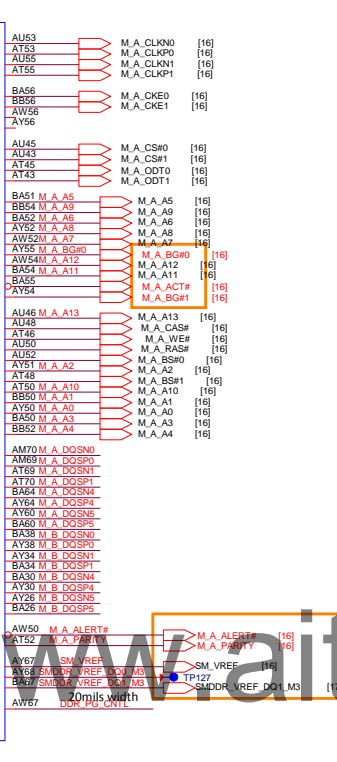
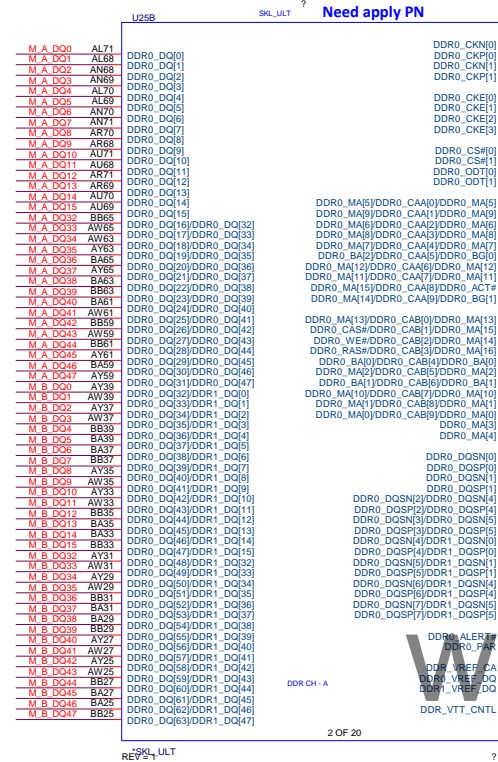
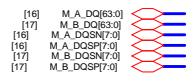
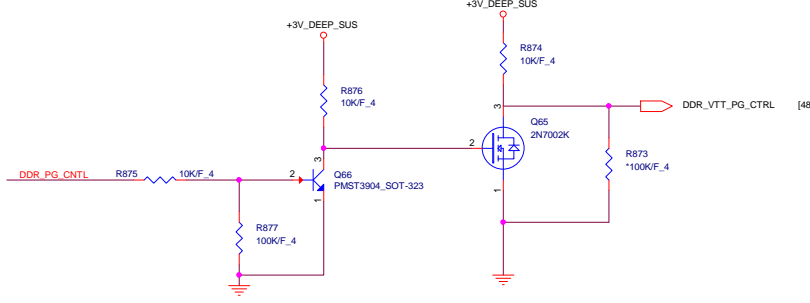
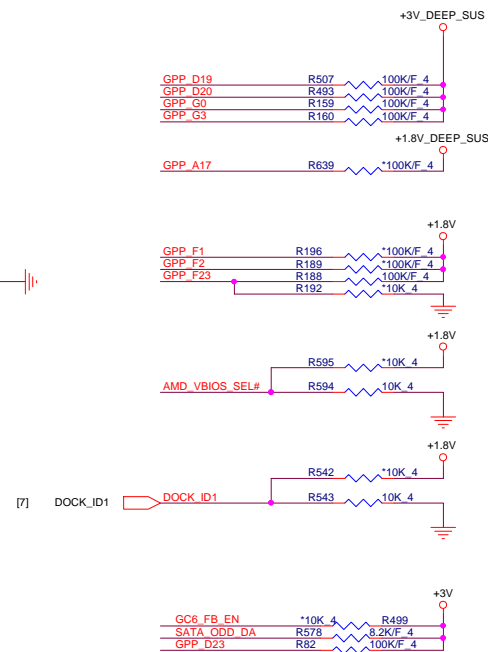


Figure 1: Schematic of the 16-bit 2D array architecture. The diagram shows a 4x4 grid of processing elements. Each element contains a 2D array of 16 bits, with a 20µs width and a 20µs height. The architecture is divided into four quadrants, each with a different color and a different set of components. The top-left quadrant (blue) contains a 4x4 array of 16 bits, with a 20µs width and a 20µs height. The top-right quadrant (orange) contains a 4x4 array of 16 bits, with a 20µs width and a 20µs height. The bottom-left quadrant (green) contains a 4x4 array of 16 bits, with a 20µs width and a 20µs height. The bottom-right quadrant (red) contains a 4x4 array of 16 bits, with a 20µs width and a 20µs height. The architecture is controlled by a 16-bit 2D array, with a 20µs width and a 20µs height. The architecture is divided into four quadrants, each with a different color and a different set of components. The top-left quadrant (blue) contains a 4x4 array of 16 bits, with a 20µs width and a 20µs height. The top-right quadrant (orange) contains a 4x4 array of 16 bits, with a 20µs width and a 20µs height. The bottom-left quadrant (green) contains a 4x4 array of 16 bits, with a 20µs width and a 20µs height. The bottom-right quadrant (red) contains a 4x4 array of 16 bits, with a 20µs width and a 20µs height. The architecture is controlled by a 16-bit 2D array, with a 20µs width and a 20µs height.

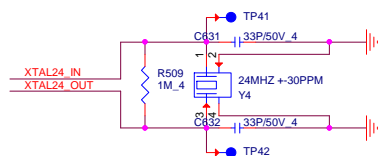
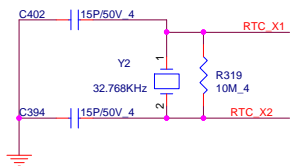




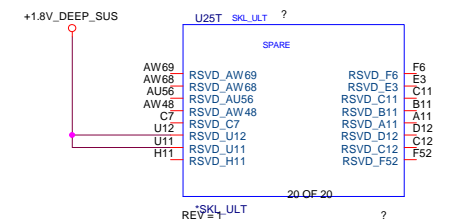
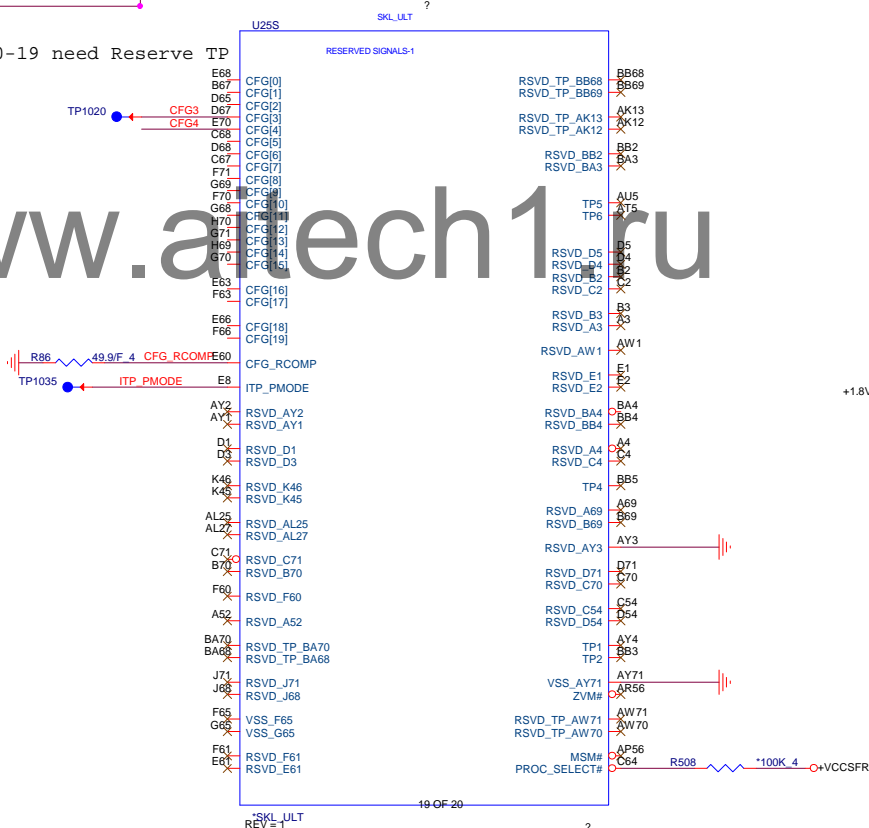
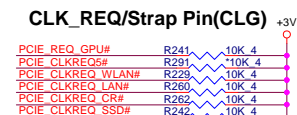
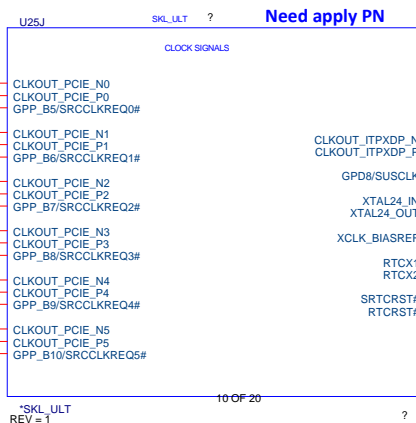
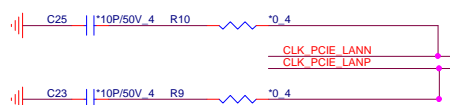
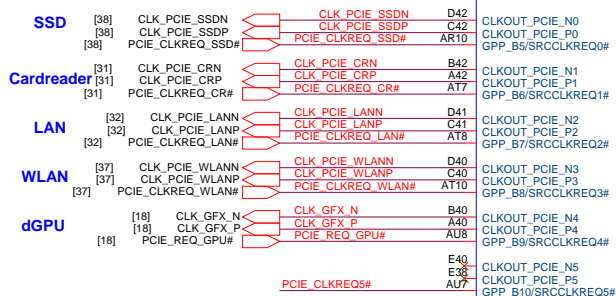
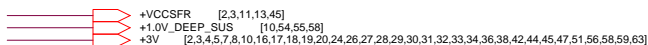
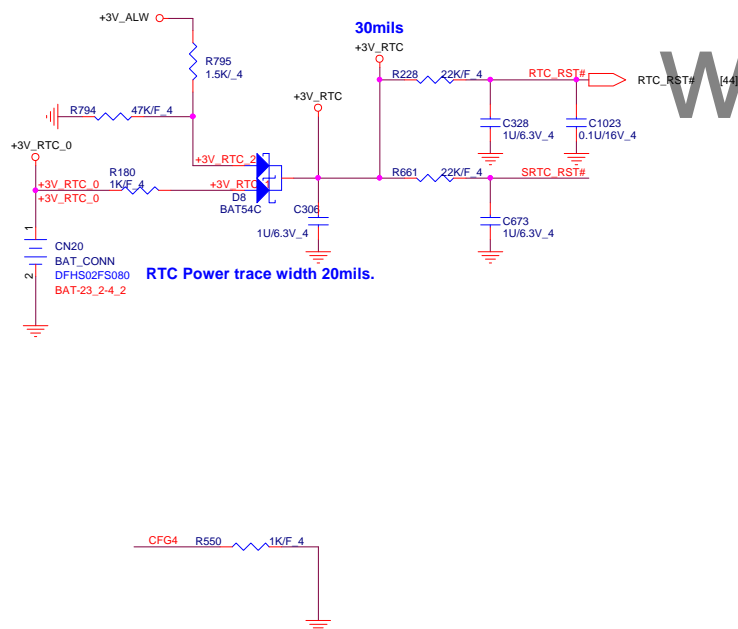


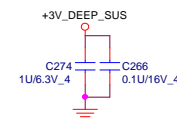
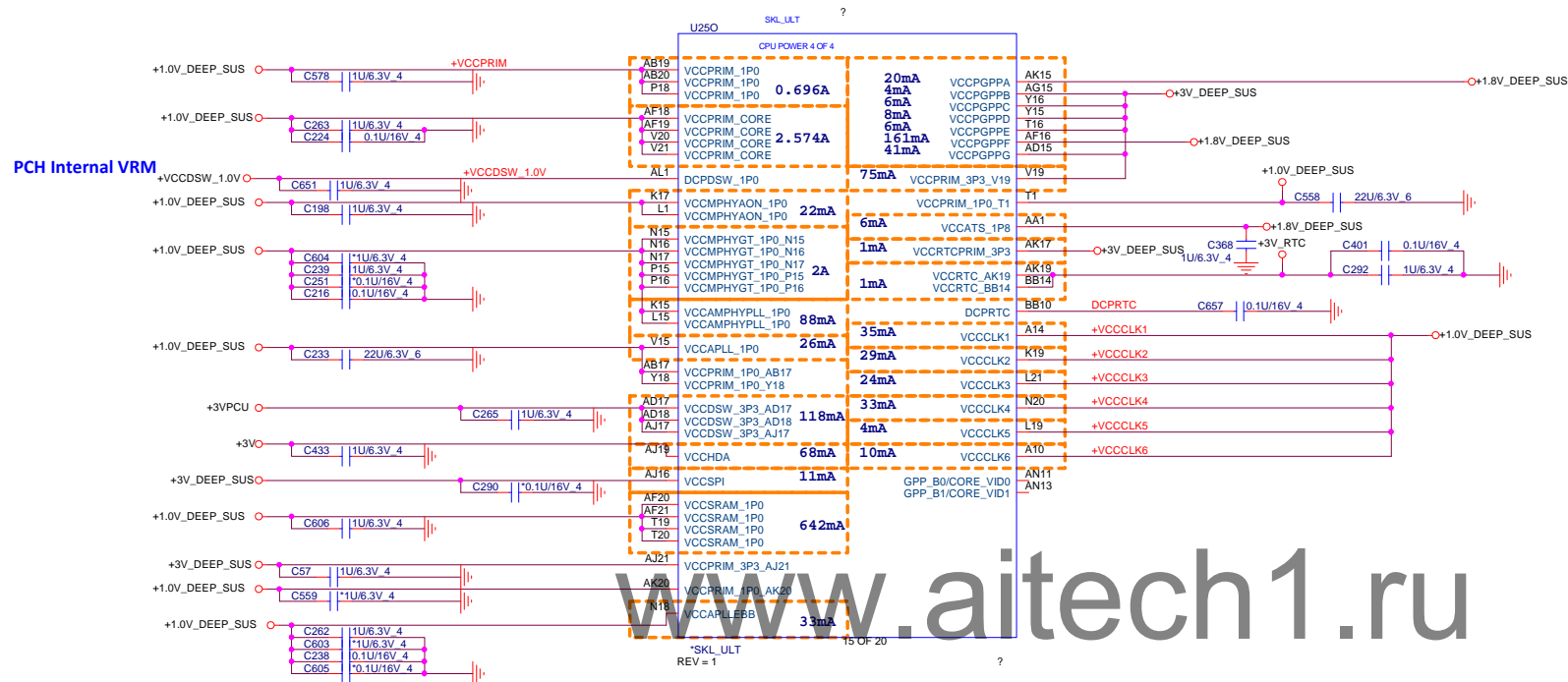
AMD_VBIOS_SEL#	DOCK_ID1
00= VBIOS 1	
01 = VBIOS 2 (Reserve for new die)	
10 = VBIOS 3 (Reserve for new die)	
11=UMA	R595,R542

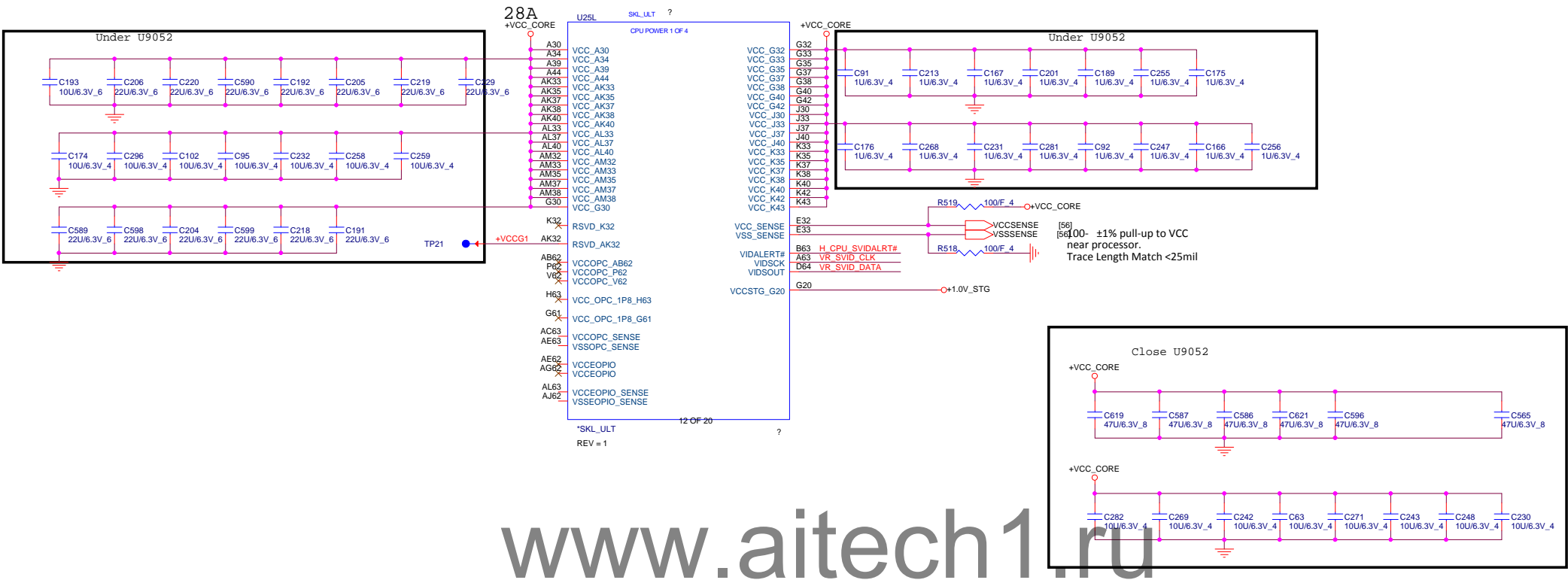
### RTC Clock 32.768KHz



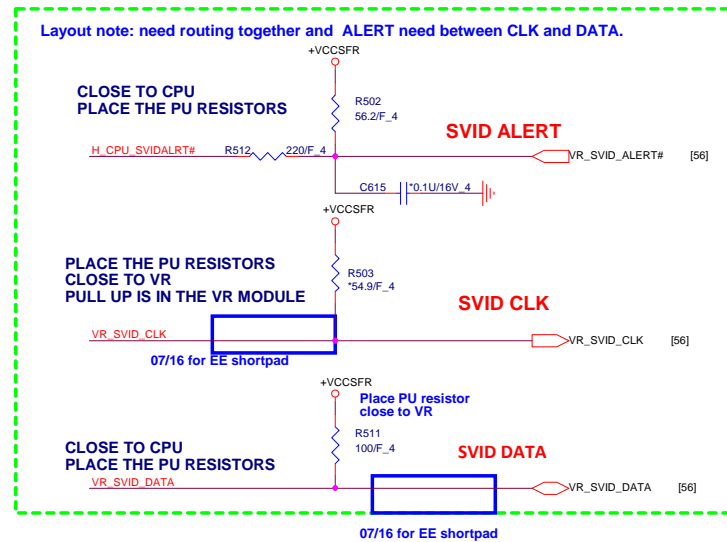
## RTC Circuitry(RTC)



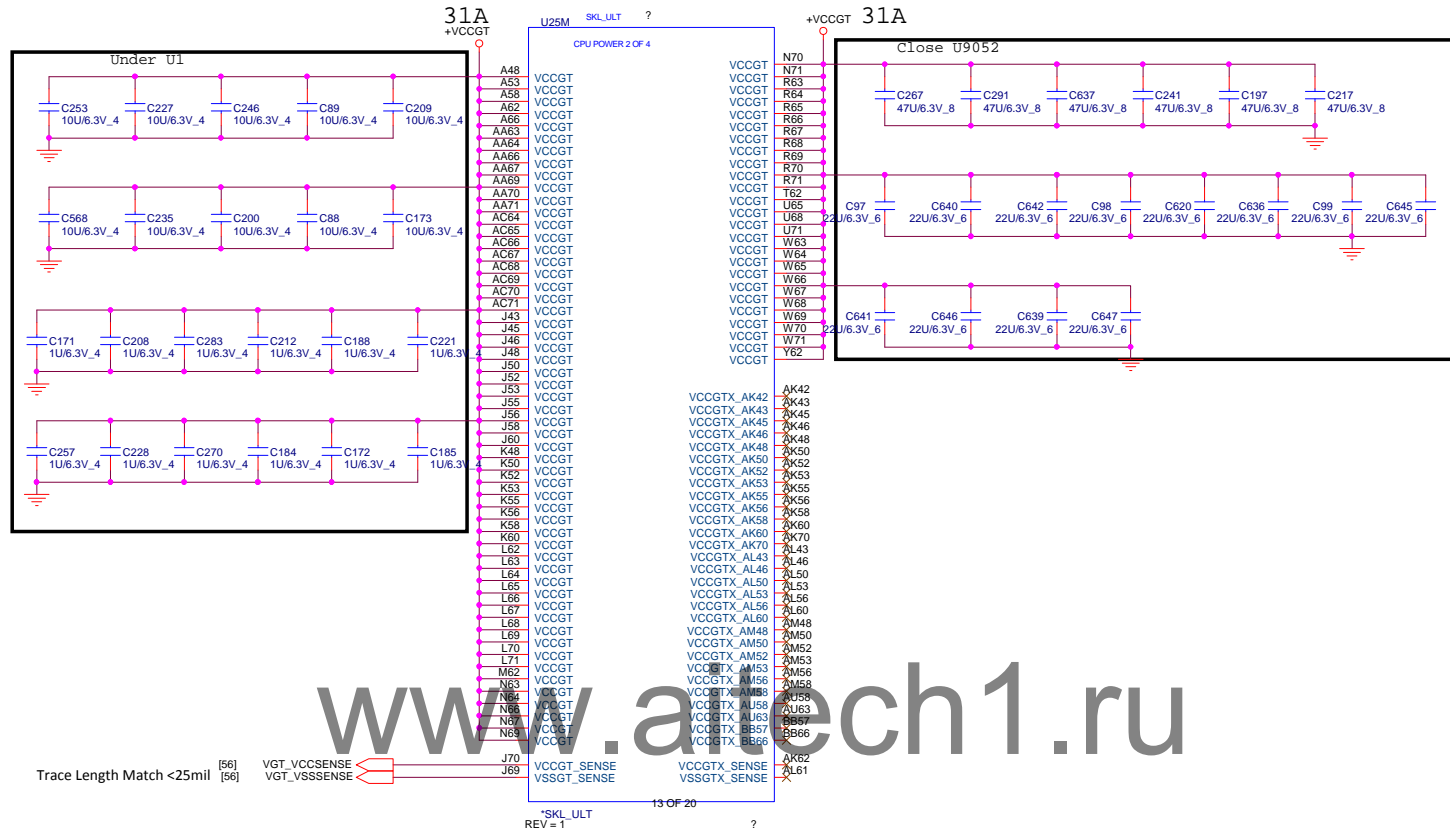




Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTX</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

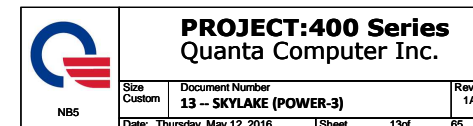


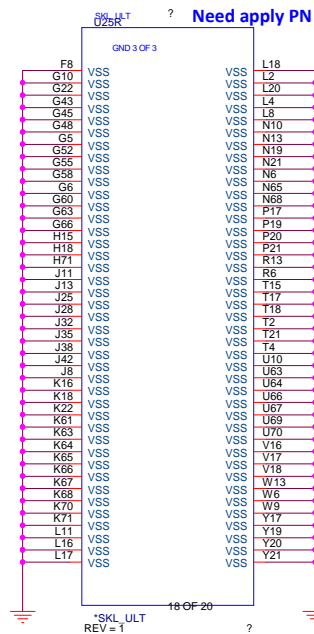




Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTx</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



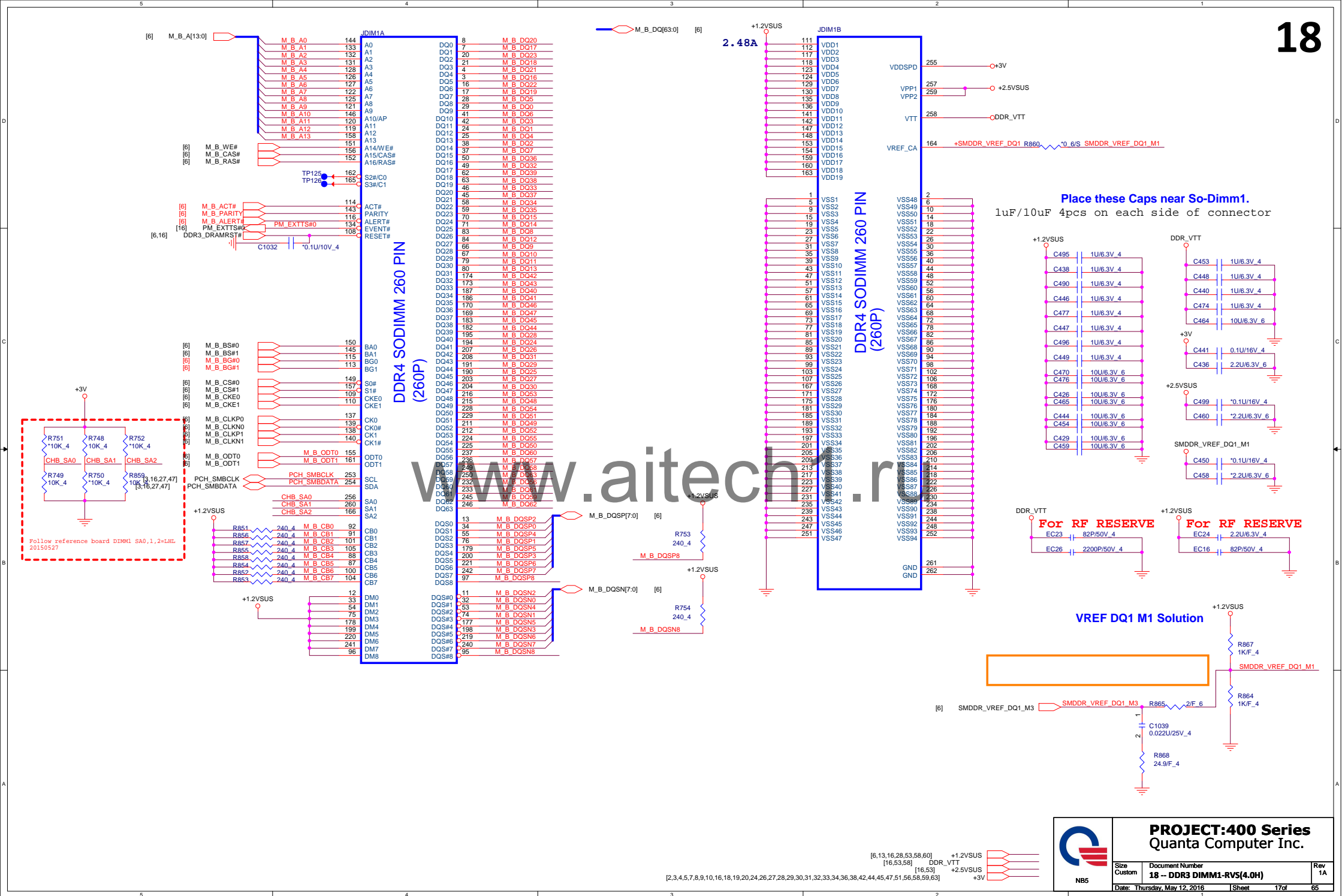


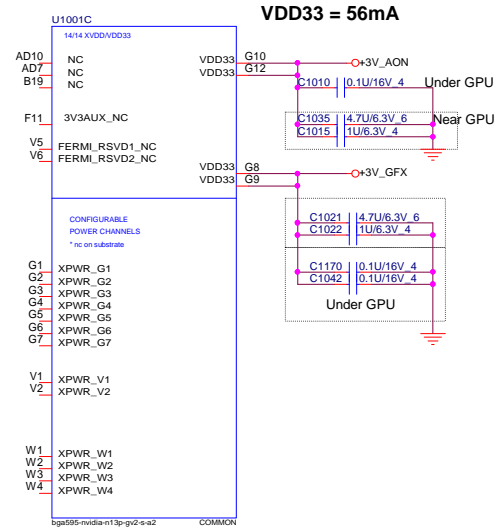
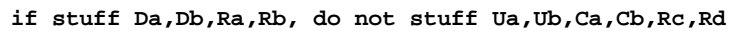
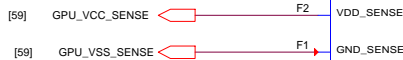


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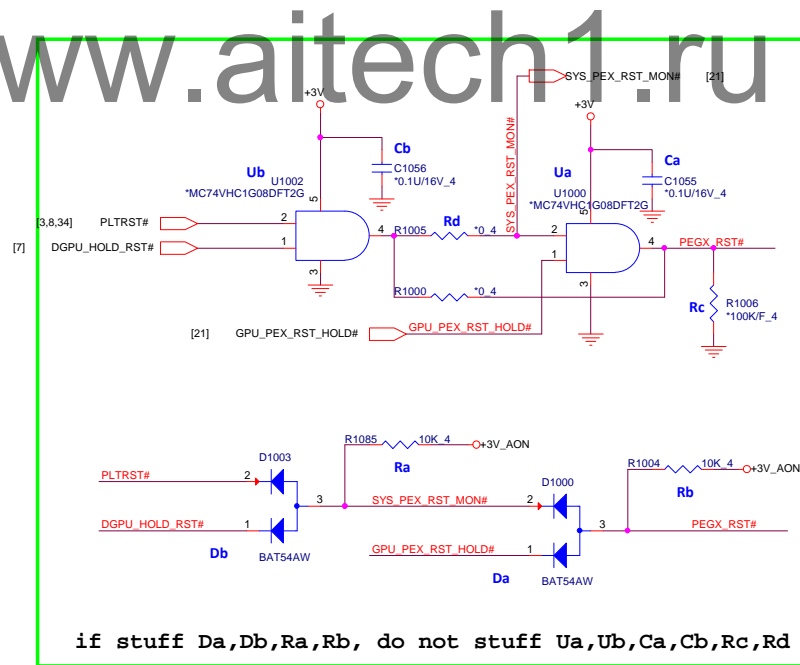
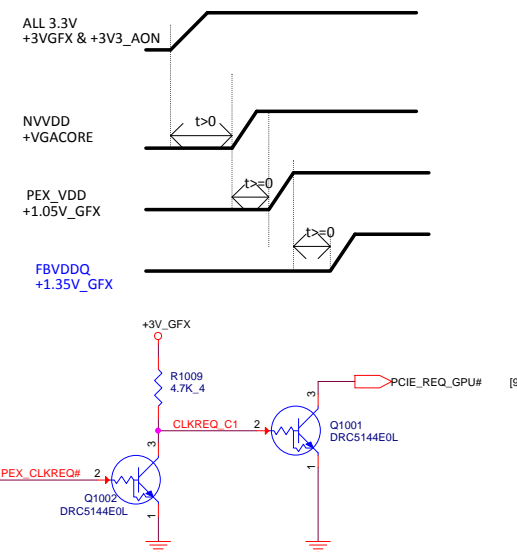
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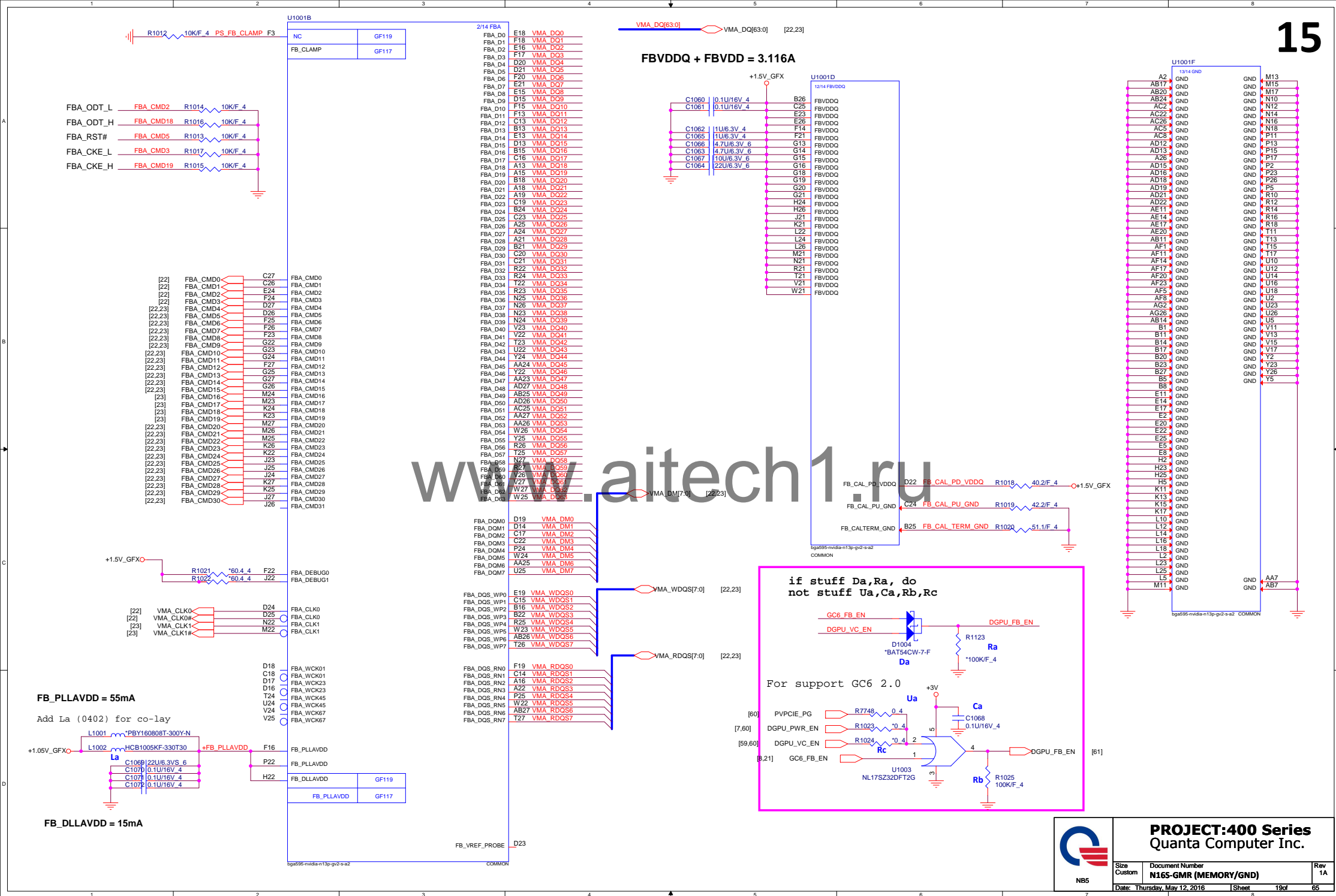




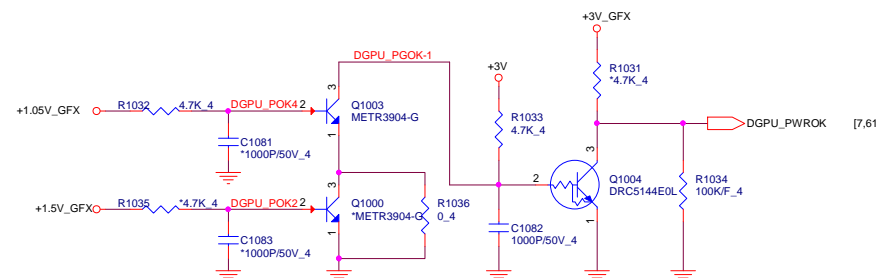


## Power up sequence

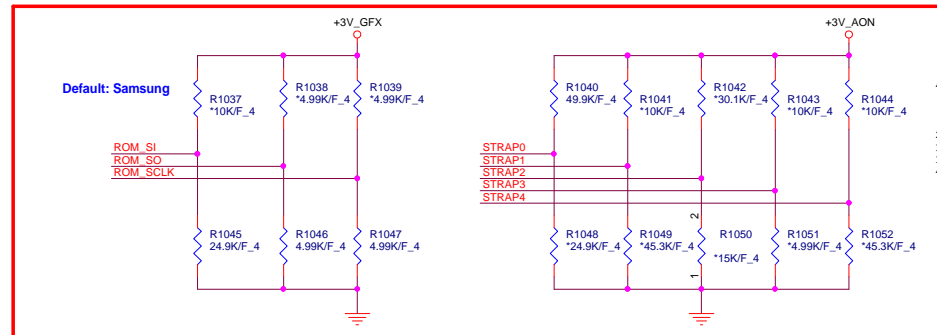
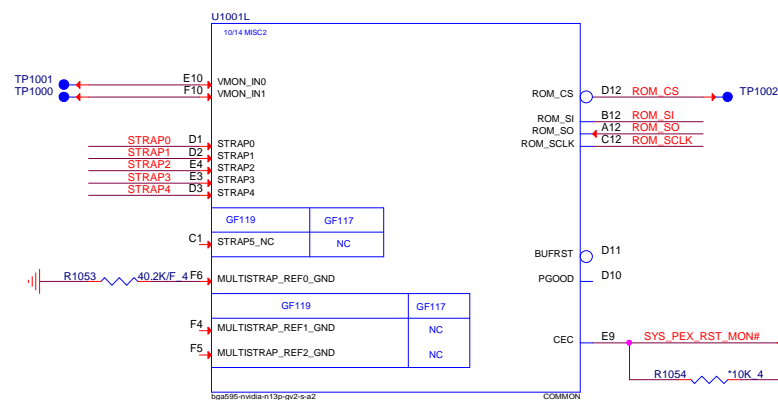








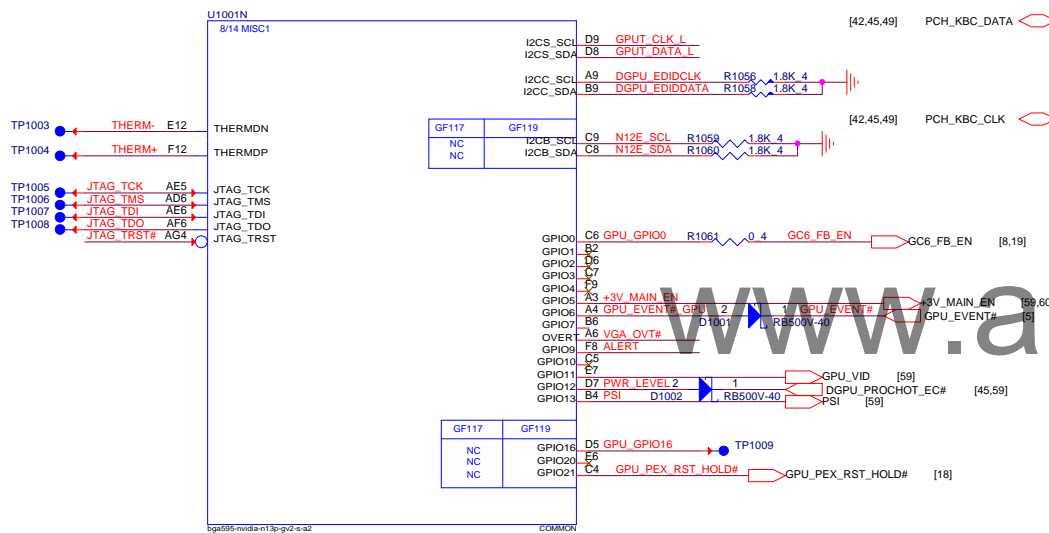




4.99k	CS24992PB26
10k	CS31002PB26
15k	CS31502PB24
20k	CS32002PB29
24.9k	CS32492PB16
30.1k	CS33012PB18
34.8k	CS33482PB06
45.3k	CS34532PB18

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111



VRAM Configuration Table

ROM SI	DESCRIPTION	Vendor	Vendor P/N	Strapping	TOP B/S	QBC
0000	DDR3 - 256Mx16, 1.5V, 1.1Ghz/1.35V 1Ghz	HYNIX	H5TC4G63CFR-N0C	0x5	AKD5PZDTW01	AKD5PZDTW02
0101	DDR3 - 256Mx16, 1.5V, 1.1Ghz/1.35V 1Ghz	Micron	MT41J256M16LY-091G:N	0x3	AKD59GSTL01	AKD59GSTL00
0100	DDR3 - 256Mx16, 1.5V, 1Ghz/1.35V 900Mhz	SAMSUNG	K4W4G1646E-BC1A	0x4	AKD5PGDT500	AKD5PGDT501

## GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMMORY_VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding



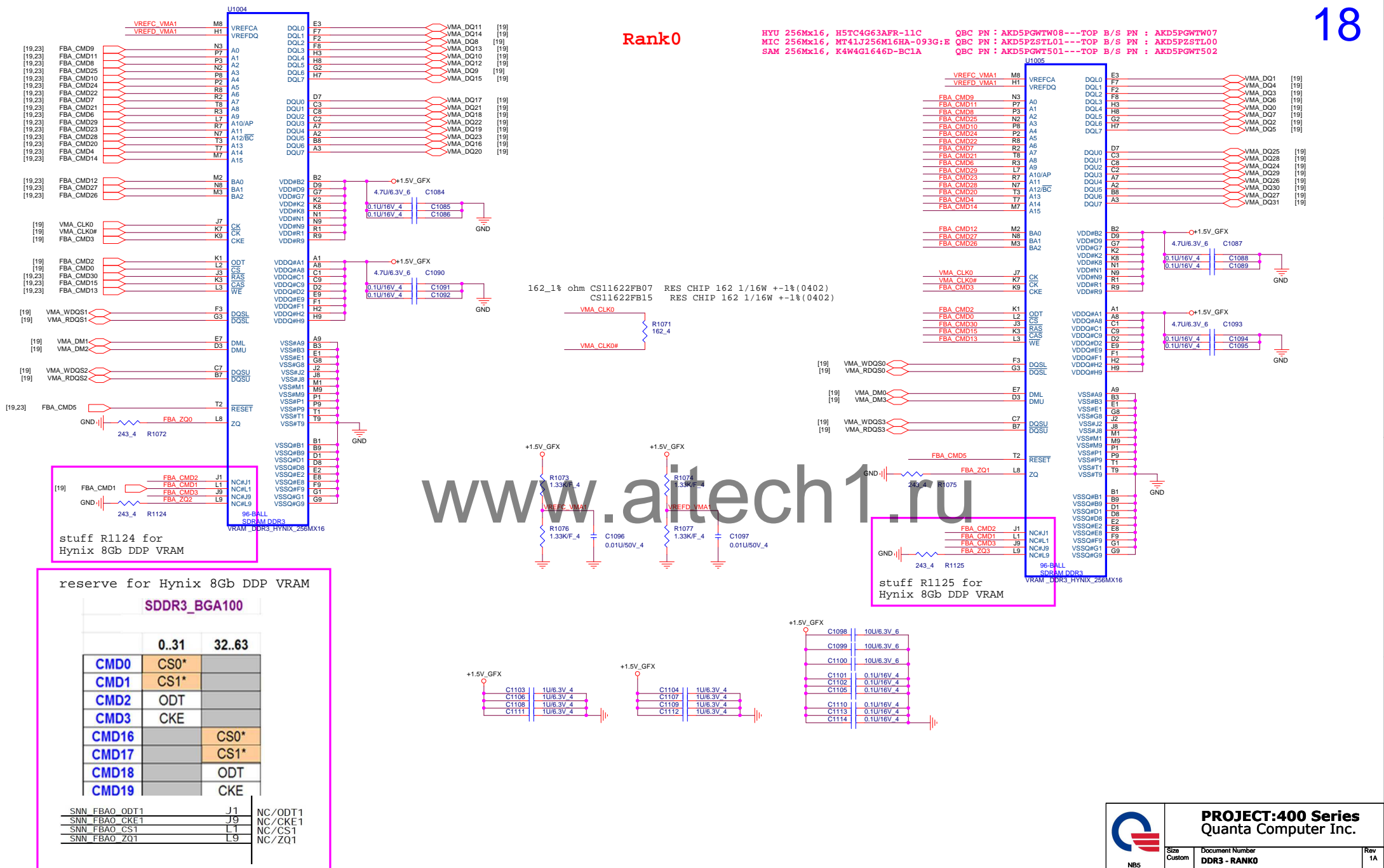
**PROJECT:400 Series**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	N16S-GMR (GPIO/STRAPS)	1A
Date: Thursday, May 12, 2016	Sheet 21 of 65	

## Rank0

HYU 256Mx16, H5TC4G63APR-11C  
MTC 256Mx16, MT41J256M16BA-093G:E  
SAM 256Mx16, K4W4G1646D-BC1A

QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07  
QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00  
QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502



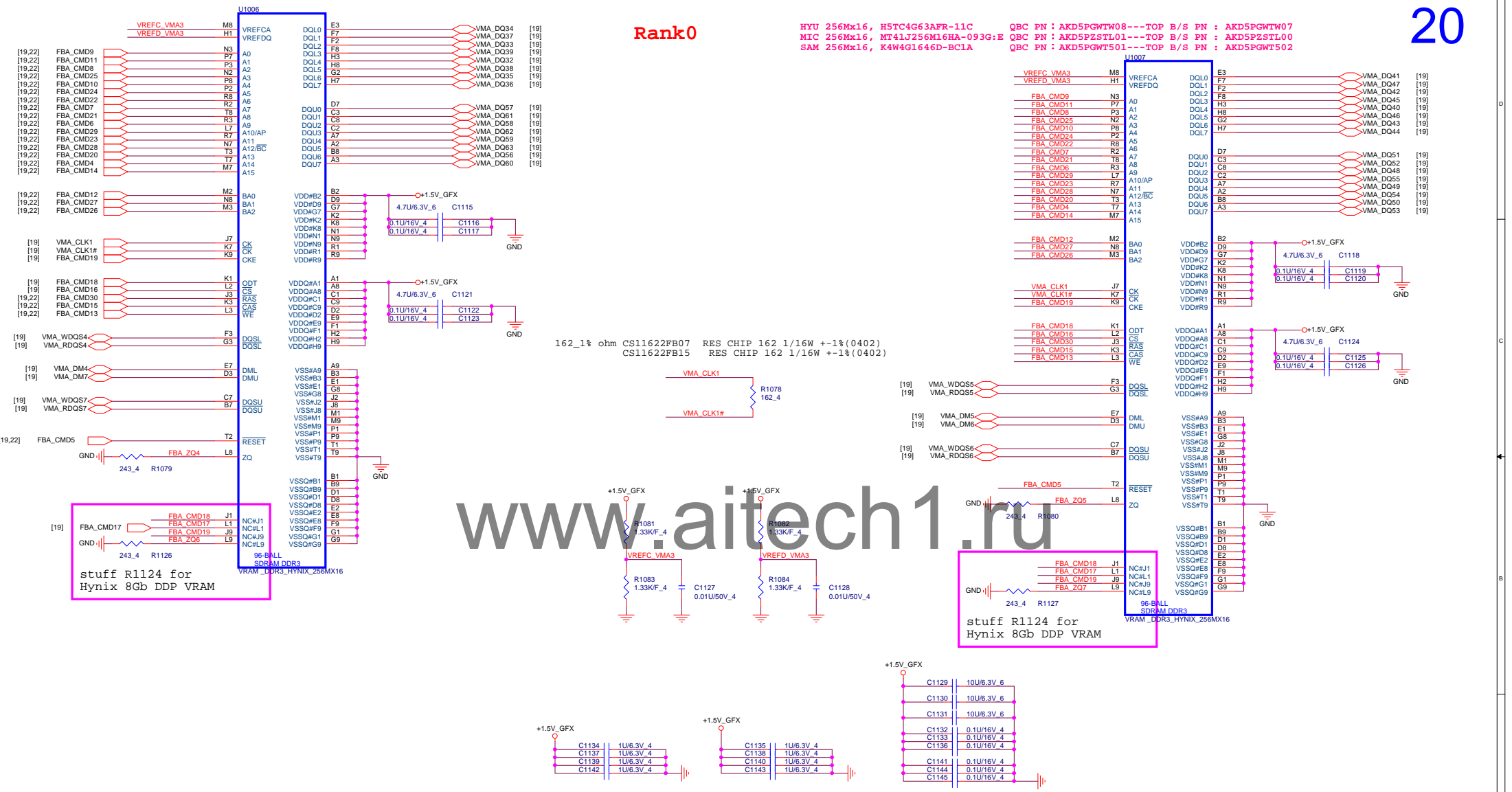
**PROJECT:400 Series**  
**DDR3 - RANK0**

Size Custom	Document Number	Rev 1A
	<b>DDR3 - RANK0</b>	
Date: Thursday, May 12, 2016	Sheet 22 of 85	

Rank0

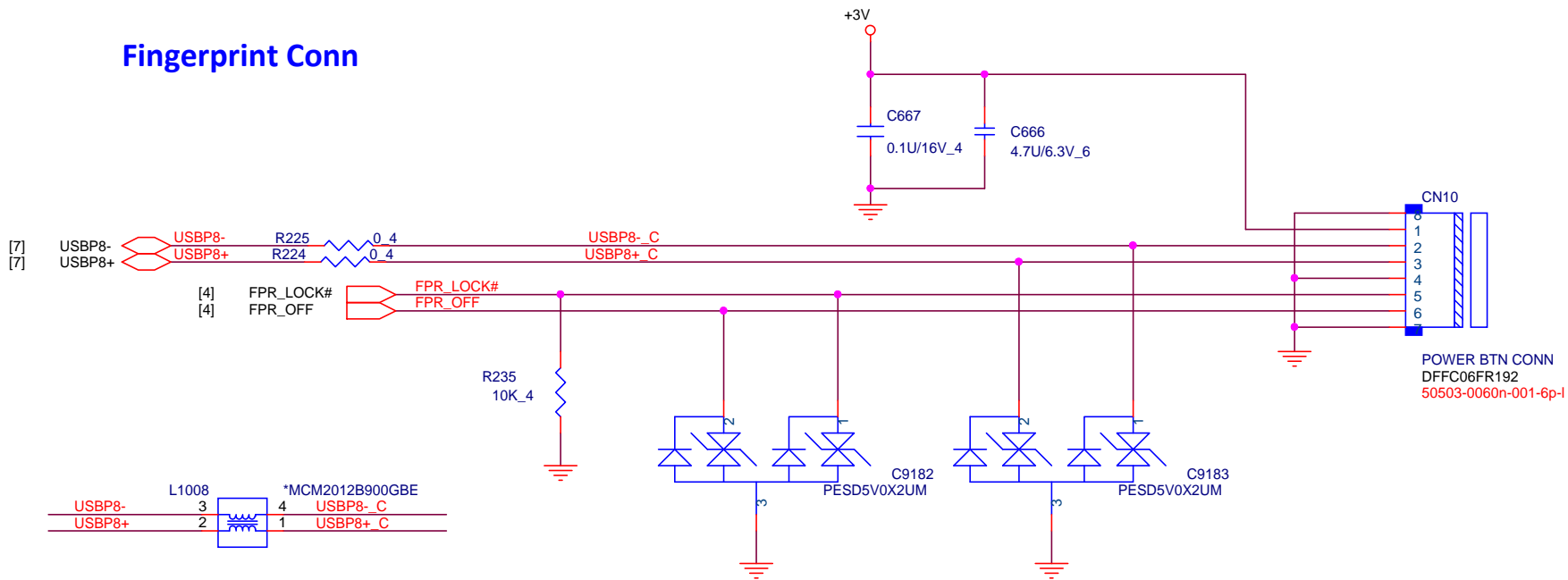
HYU 256Mx16, H5TC4G63AFR-11C  
MIC 256Mx16, MT41J256M16HA-093G:E  
SAM 256Mx16, K4W4G1646D-BC1A

QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07  
QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00  
QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502



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## Fingerprint Conn



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**PROJECT:400 Series**  
Quanta Computer Inc.

Size  
Custom

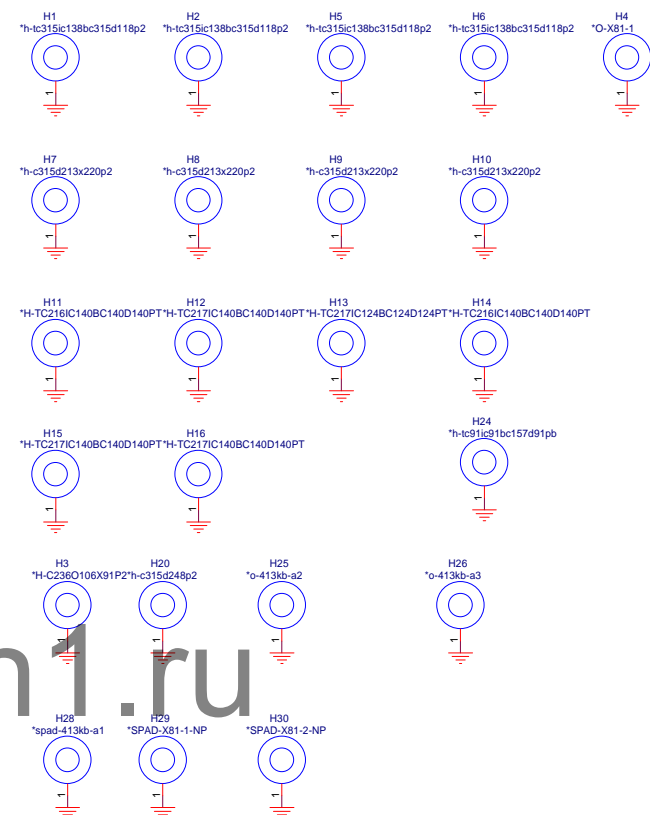
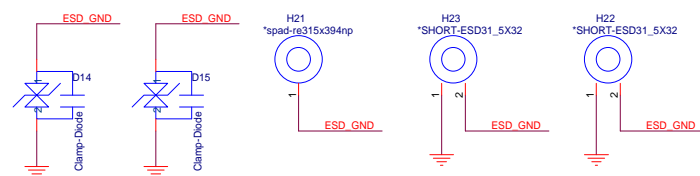
Document Number  
**24 -- FPR**

Rev  
1A

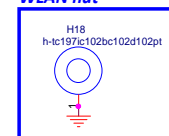
Date: Thursday, May 12, 2016

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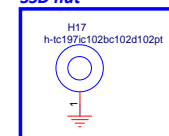
## Hole



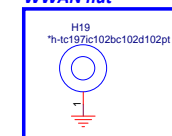
## WLAN nut



## SSD nut



## WWAN nut

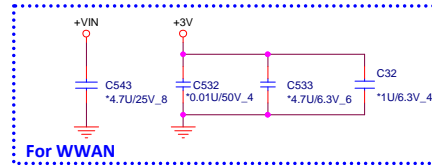
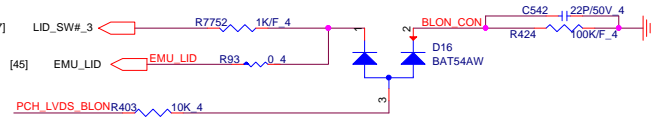


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# LID Switch

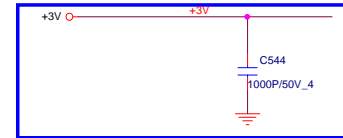
LVDS Conn.

26

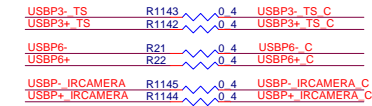
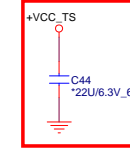
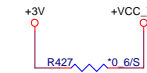
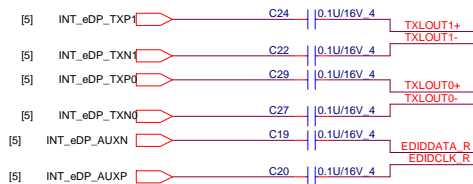
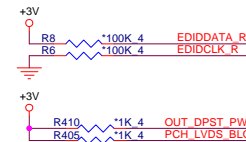
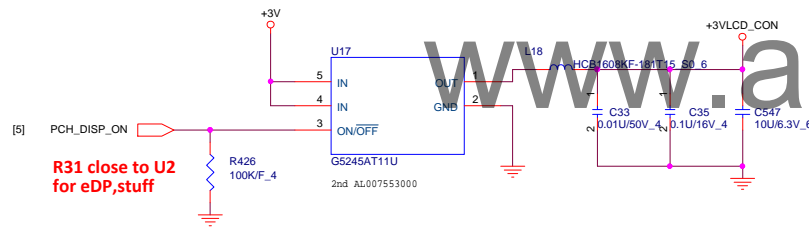


ALF@20151019:

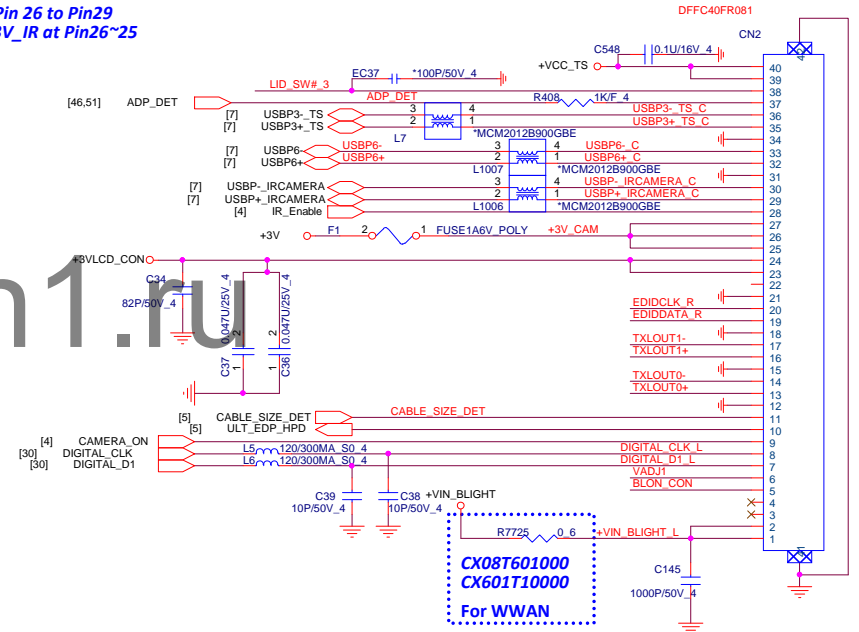
1. Designed Reserve 4Pins for IR CCD Pin 26 to Pin29
2. Combined the +3V & +3V\_CAM & +3V\_IR at Pin26~25



For eDP  
Close to LVDS connector



GS12401-1011-9H  
lvs-50671-04041-001-40p-I

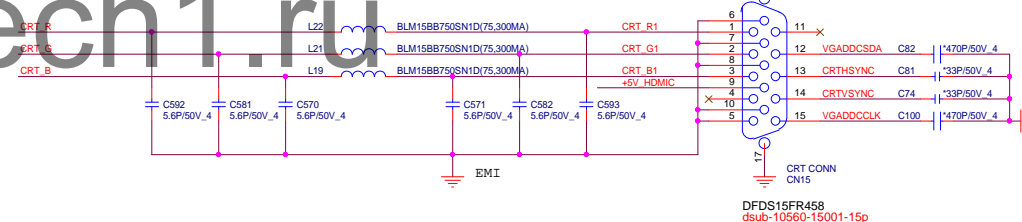
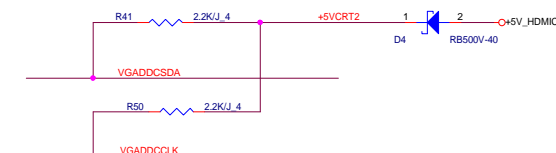


For WWAN



PROJECT:400 Series  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	26 - LCD CONN/LID/CAM/D-MIC	1A
Date: Thursday, May 12, 2016	Sheet 26 of 65	

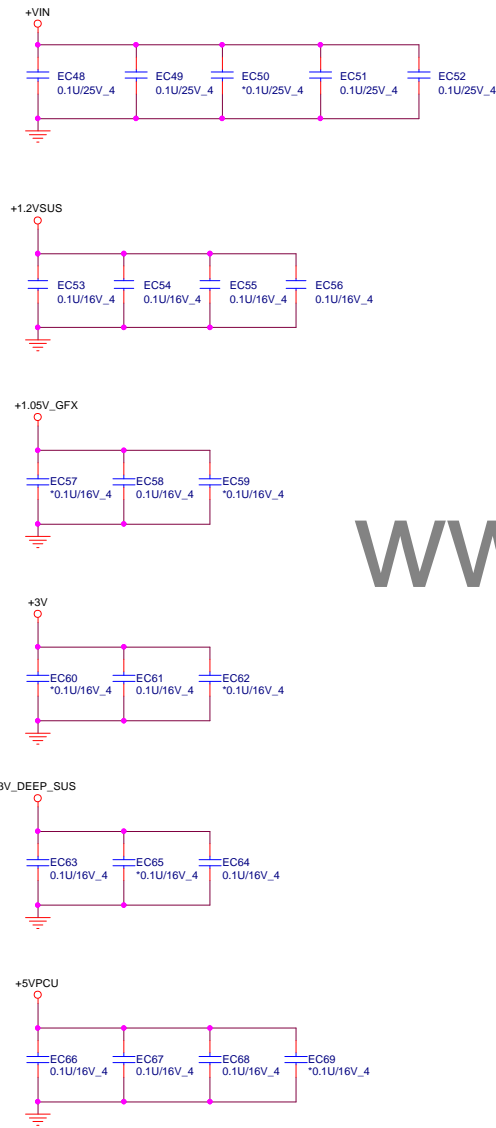


EP mode: Pin2, Pin3 connect to EC SMBUS  
ROM or EEPROM mode: connect to PCH SMBUS  
IIC Protocol is used

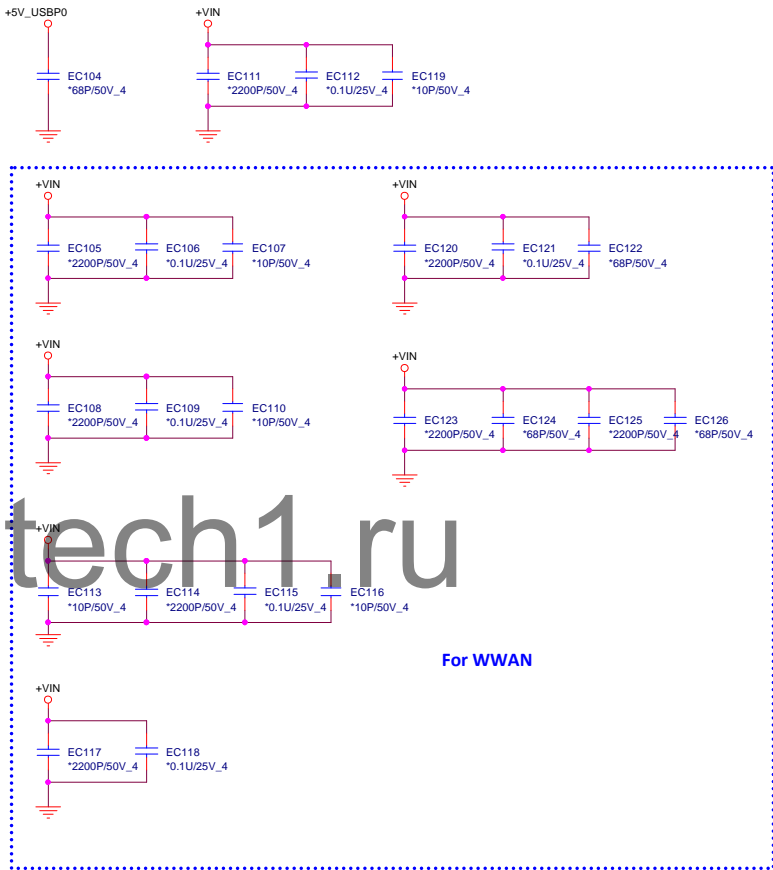
**From PCH**



EMI CAP



RF Cap



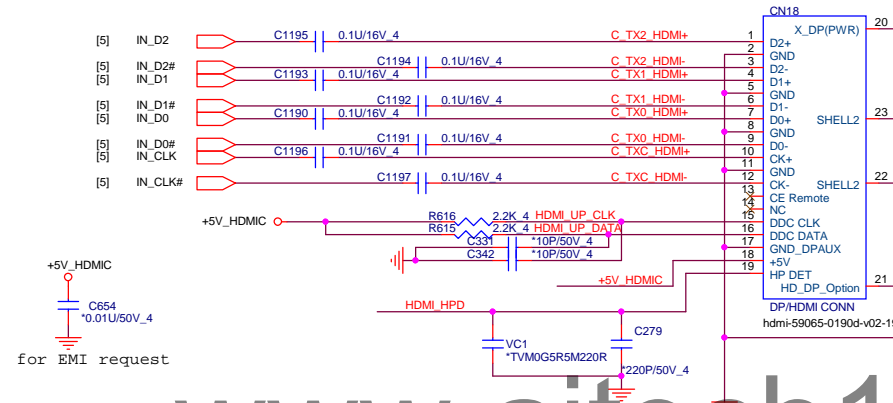
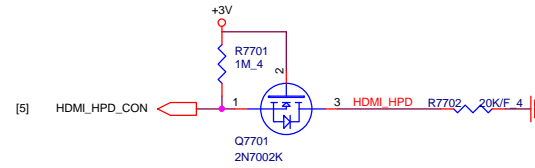
For WWAN

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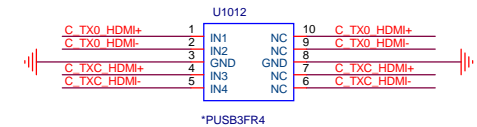
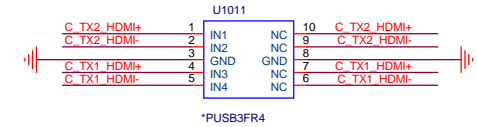
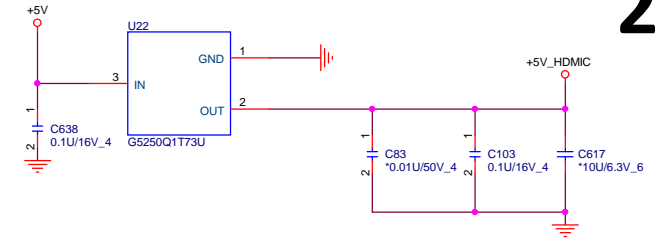


## EMI Solution

C_TX2_HDMI+	R208	120/F 4	C_TX2_HDMI-
C_TX1_HDMI+	R194	120/F 4	C_TX1_HDMI-
C_TX0_HDMI+	R178	120/F 4	C_TX0_HDMI-
C_TXC_HDMI+	R221	120/F 4	C_TXC_HDMI-

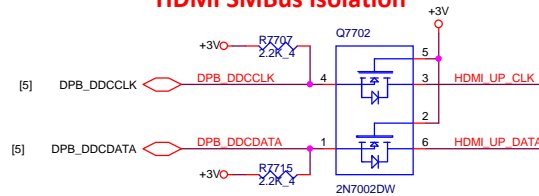


for EMI request

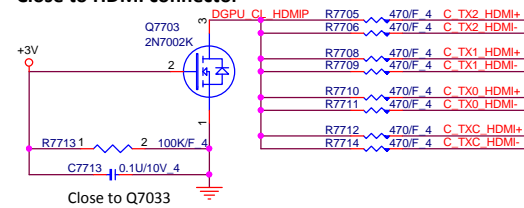


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## HDMI SMBus Isolation

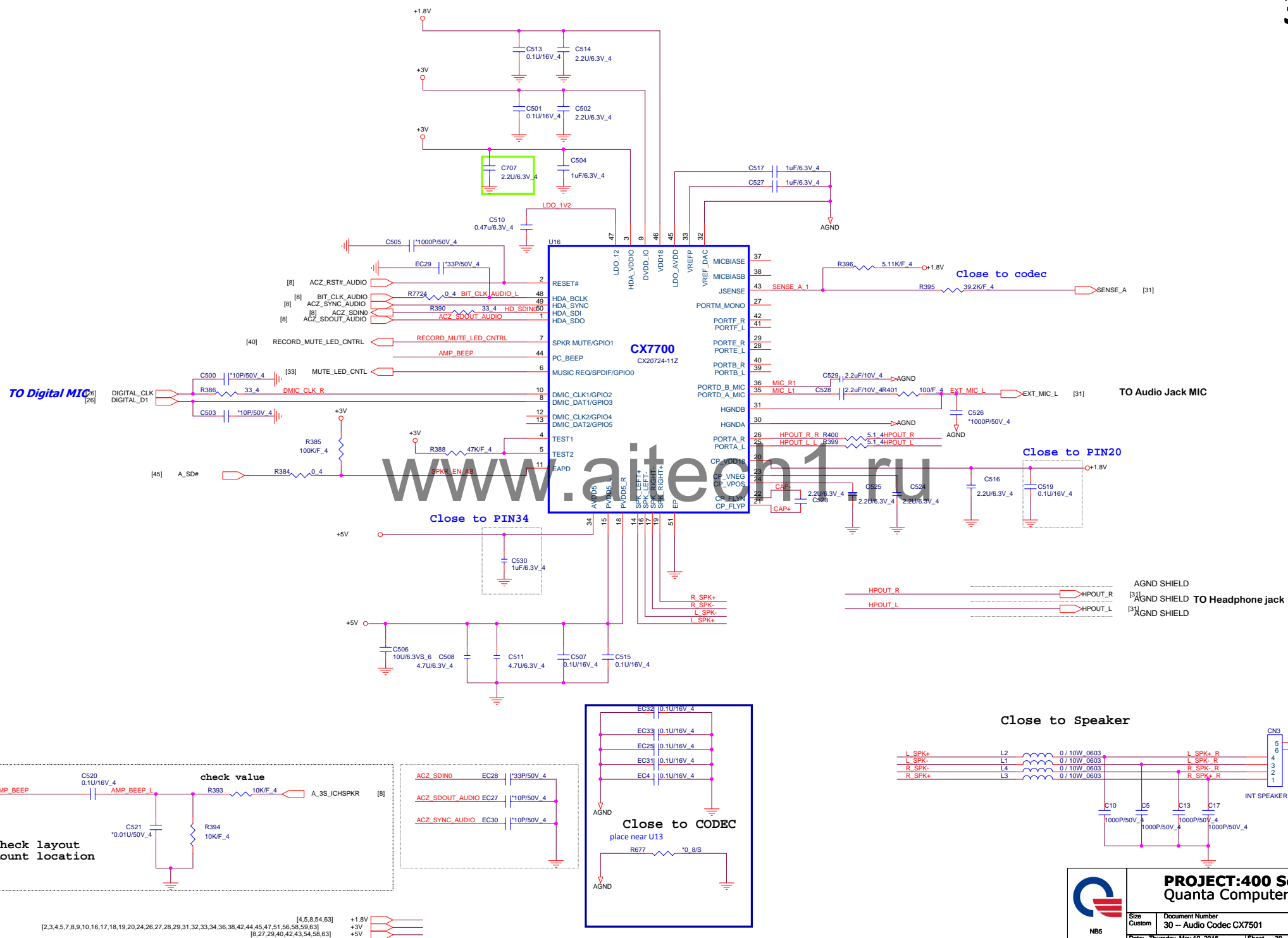


## Close to HDMI connector

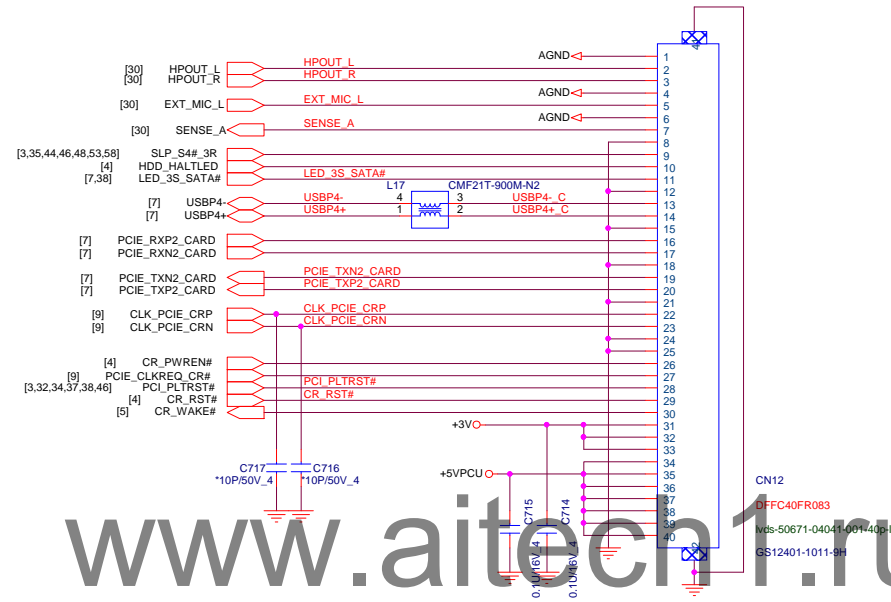



**PROJECT:400 Series**  
Quanta Computer Inc.

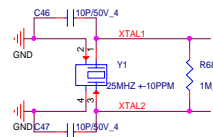
Size Custom	Document Number	Rev 1A
	<b>29 -- HDMI CONNECTOR</b>	
Date: Thursday, May 12, 2016	Sheet 29 of 65	



# USB/Card Reader/Headphone\_Mic Combo Jack Daughter Board Connector



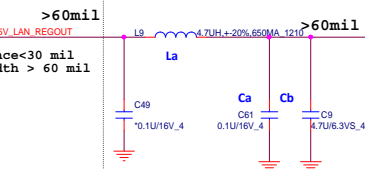
 NB5	<b>PROJECT:400 Series</b> Quanta Computer Inc.		
	Size Custom	Document Number 31 -- DAUGHTER BOARD CONN.	Rev 1A
Date: Thursday, May 12, 2016 Sheet 31 of 65			



### Power trace Layout 寬度> 60mil

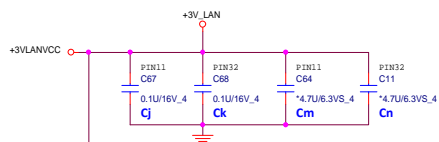
\* Place Cc,Cd,Ce,Cf  
close to each VDD10 pin-- 3, 22, 8, 30

\* Place Cg,Ch  
close to each VDD10 pin-- 22(reserved)



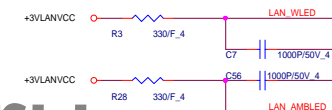
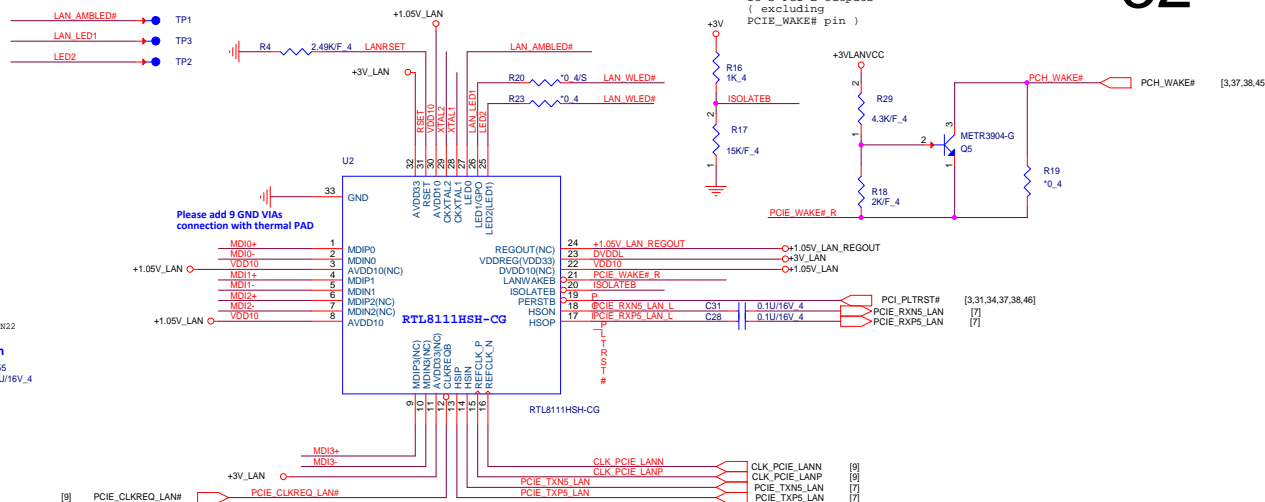
For SWR mode  
 Stuff La, Ca ,Cb  
 NA : Ra, Ci

- \* Place Cj and Ck, close to each VDD33 pin-- 11, 32
- \* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)

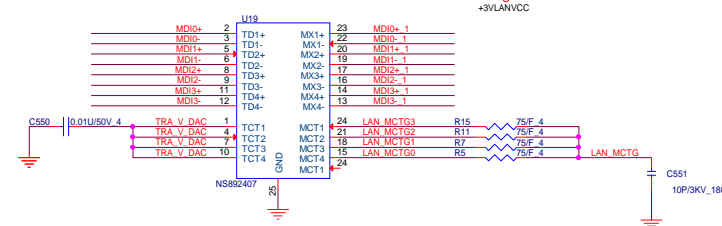
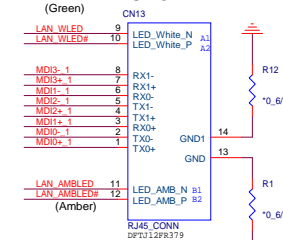


For SWR mode  
Stuff Co, Cp

**Remove For Not Using SWR mode**



RJ45

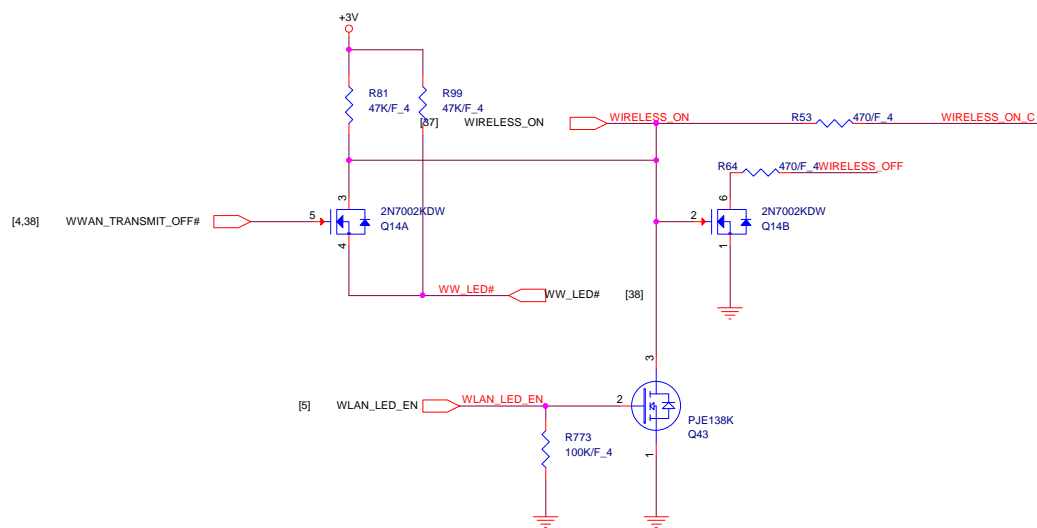
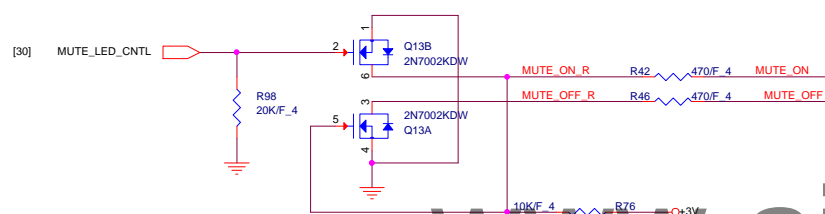
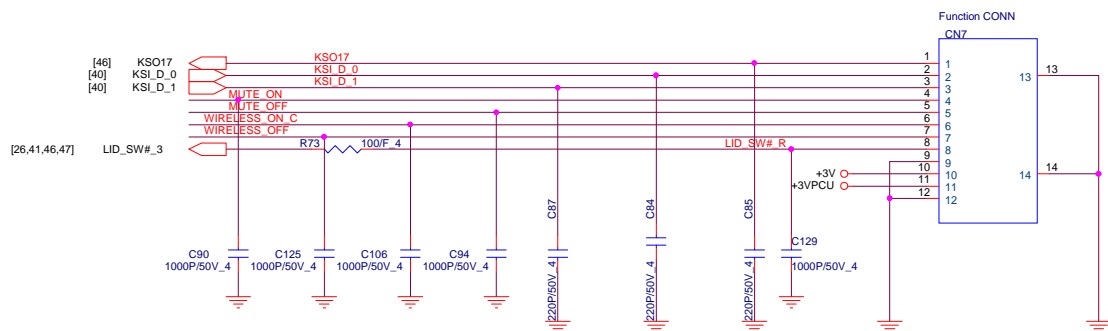


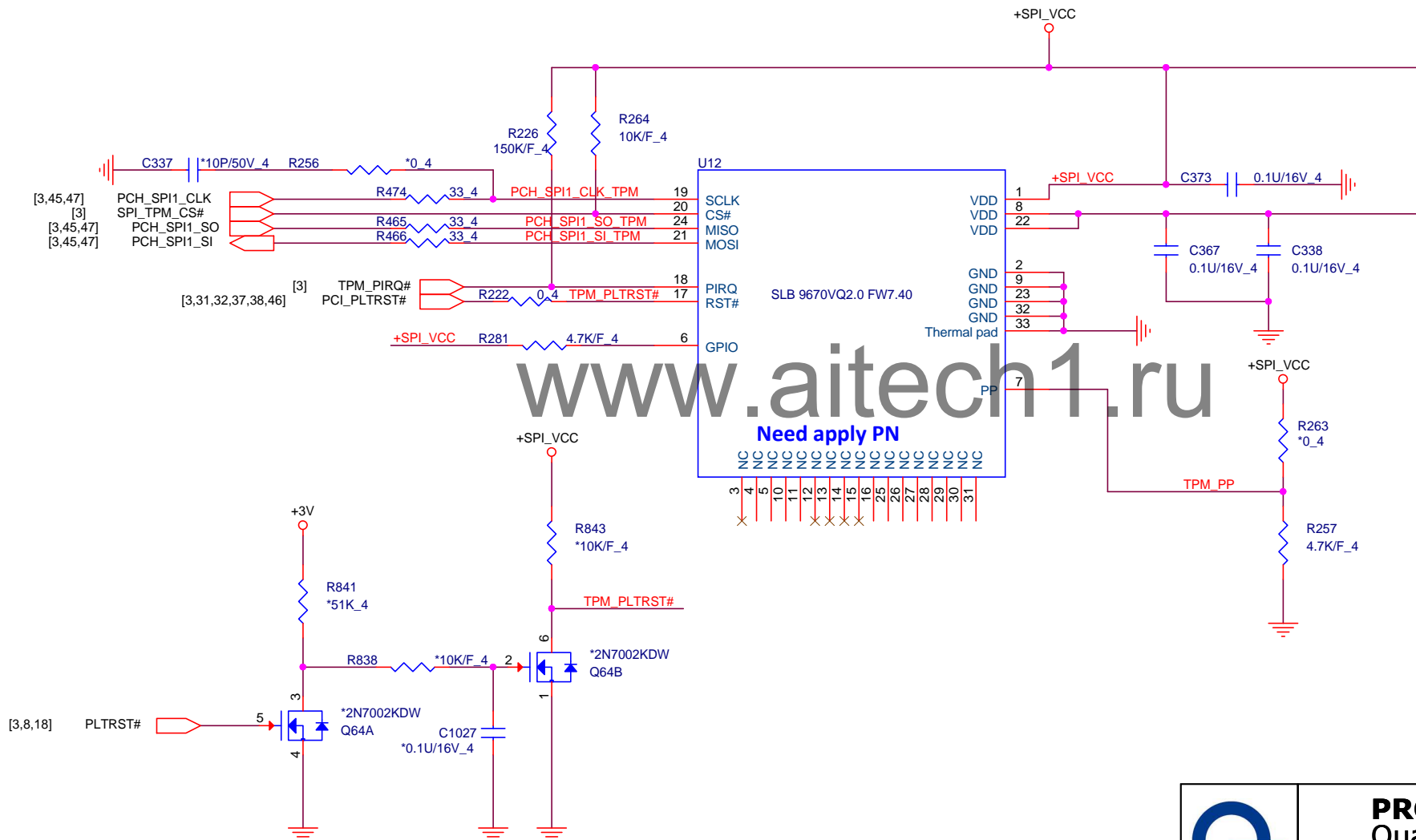
For GiGA BOT:GST5009B LE DB0Z06LAN00

FCE :NS892407 ,DB0LL1LAN00

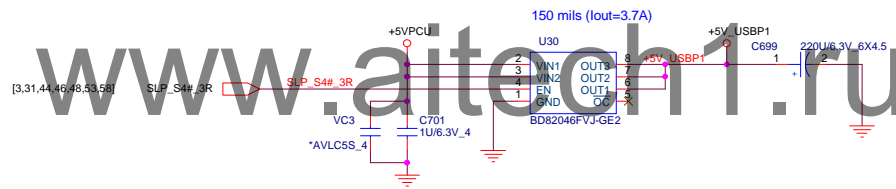
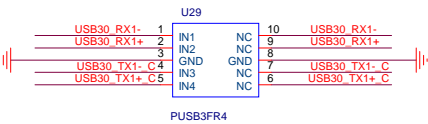
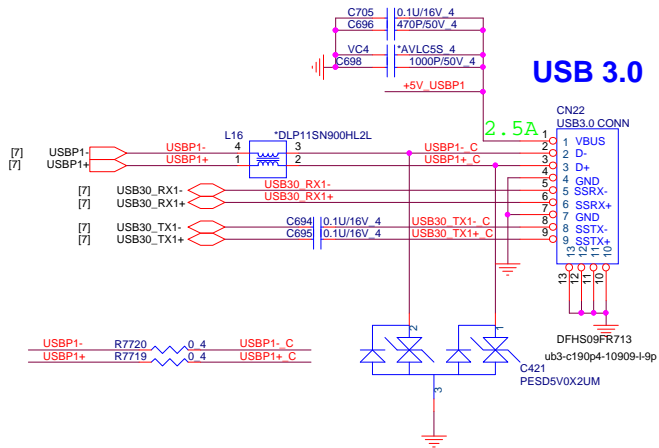
[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,33,34,36,38,42,44,45,47,51,56,58,59,63]

[58] +3V  
+3VLANVCC





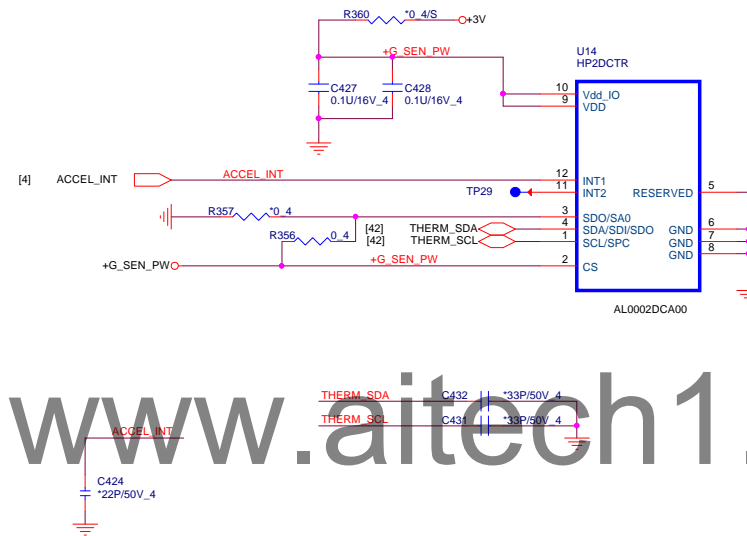
# USB 2.0/3.0 Combo



[28,31,44,49,50,51,52,53,54,56,57,58,59,60,61,63] +5VPCU

[3,10,33,37,38,40,41,42,44,45,46,48,49,51,52,53,55,58,60,62,63] +3VPCU

## Accelerometer Sensor



[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,38,42,44,45,47,51,56,58,59,63]

+3V 

[3,10,33,37,38,40,41,42,44,45,46,48,49,51,52,53,55,58,60,62,63]

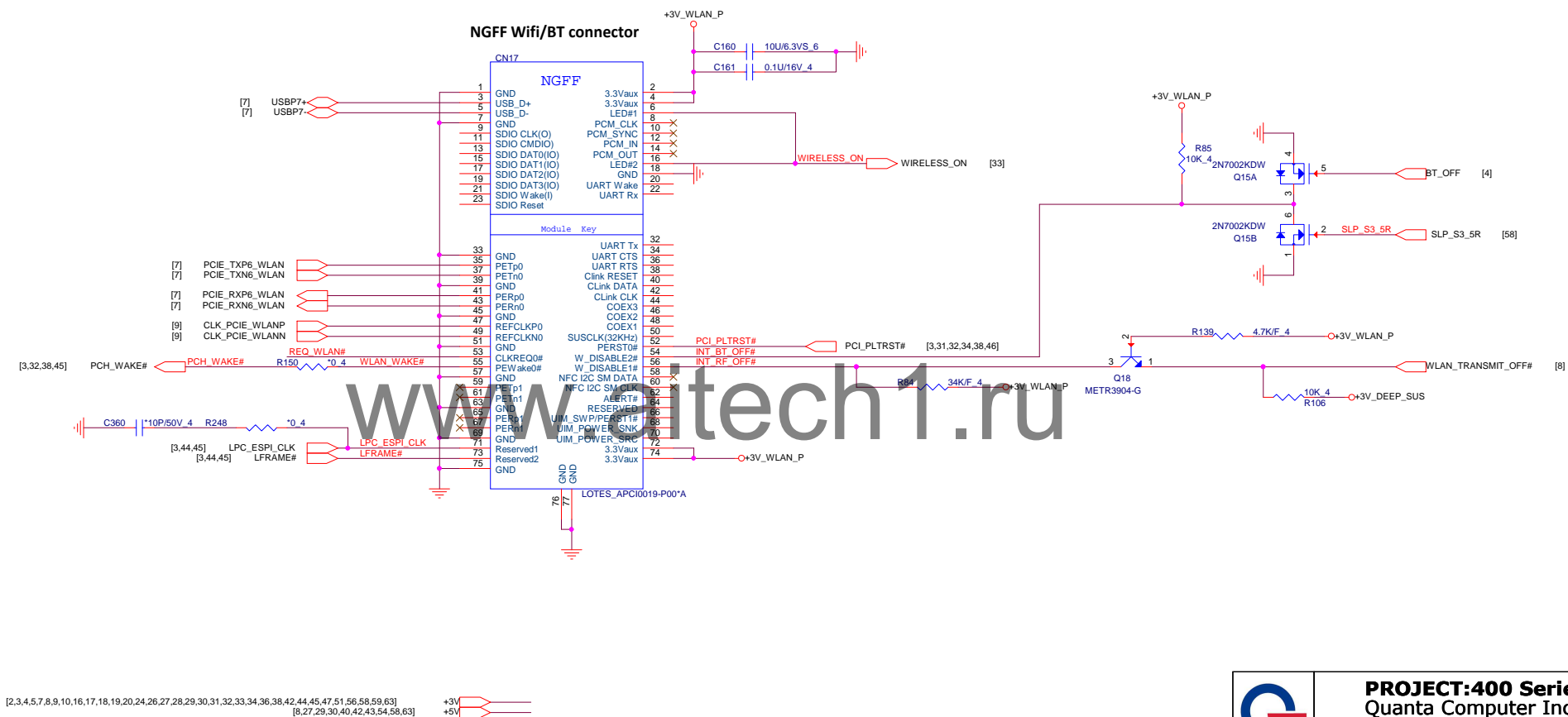
+3VPCU 

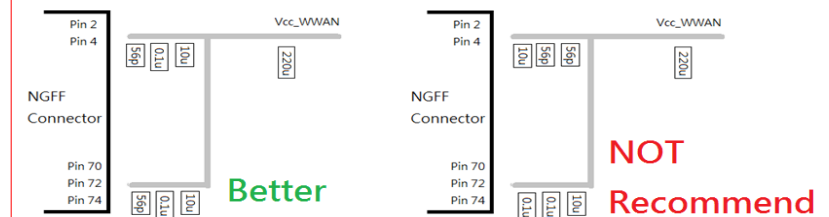
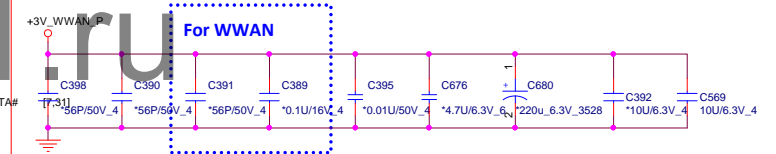
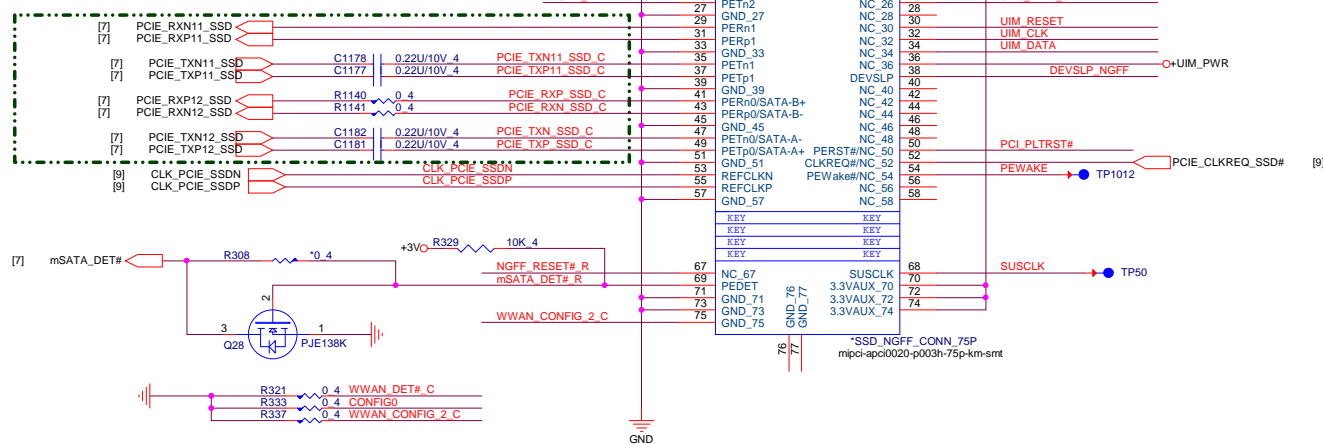
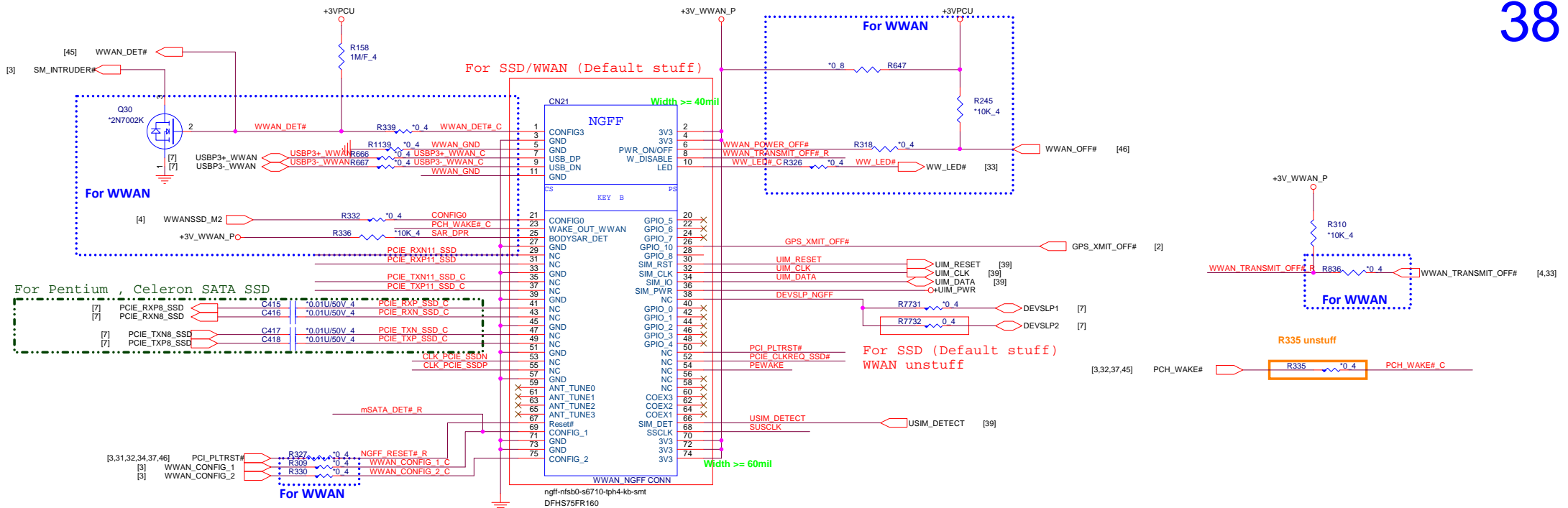


**PROJECT:400 Series**  
Quanta Computer Inc.

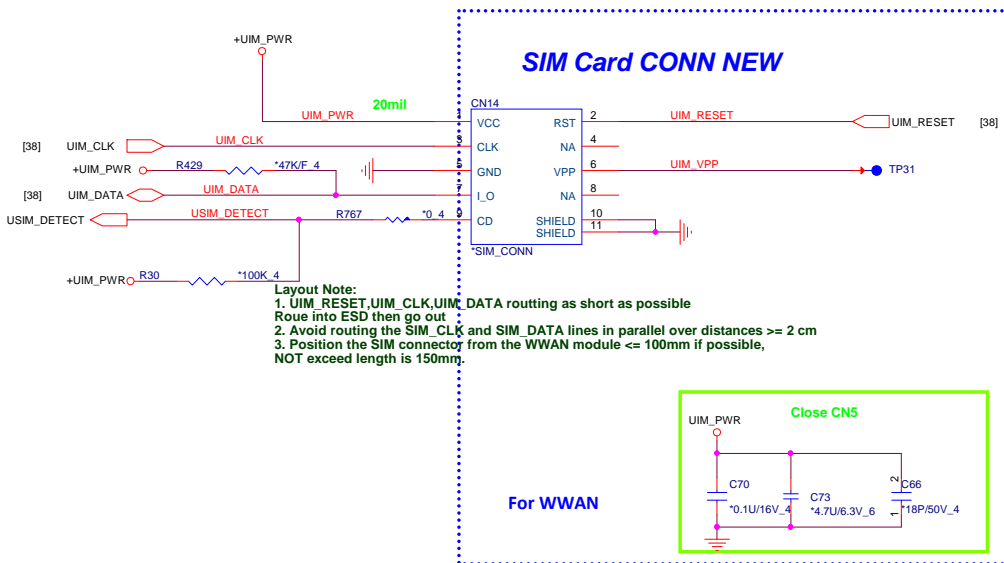
Size Custom	Document Number <b>36 -- TS and Accelerometer</b>	Rev 1A
Date: Thursday, May 12, 2016	Sheet 36 of	65







+VCC	Power_On/Off (Pin6)	W_Disable (Pin8)	GPS_Disable (Pin26)
S0 ON	High	High	High
S3 ON	High	Low	Low
S4 ON	Low	Low	Low
S5 ON	Low	Low	Low

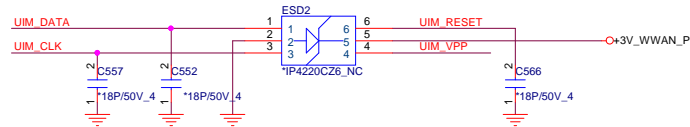


#### Trace Length and Routing<sup>u</sup>

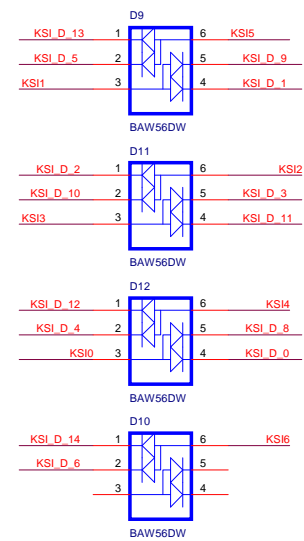
- Special attention should be paid to SIM traces (UIM\_CLK, UIM\_DATA and UIM\_RST) to minimize the trace lengths between the SIM slot and the WAN NGFF slot. **Minimizing the signal lengths and traces will reduce possibility of SIM signal integrity issues.** Recommended maximum length is 100mm. Not to exceed length is 150mm.<sup>u</sup>
- Minimum distance between UIM\_CLK and UIM\_DATA should be 20 mils. Static signals such as UIM\_RST can be routed between UIM\_CLK and UIM\_DATA to conserve space if needed.<sup>u</sup>
- It is recommended that SIM traces be isolated from other high-speed switching signals, as noise can couple into the SIM signals. Keep a minimum distance of 20 mils between UIM\_CLK, UIM\_DATA and any other high-speed switching signals.<sup>u</sup>
- Placing the SIM card on a daughter card is also not recommended as the interconnect may impact SIM signal integrity.<sup>u</sup>

#### SIM Power<sup>u</sup>

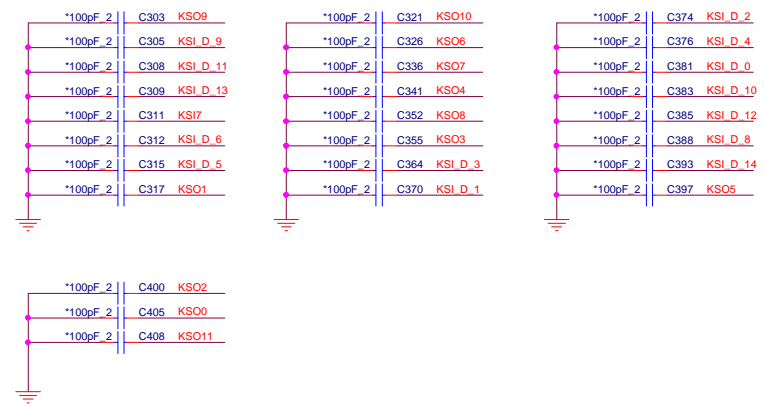
- The UIM\_PWR trace width must be at least 20 mils. Sub-planar routing is recommended.<sup>u</sup>
- Implement additional power filtering to SIM card power to ensure clean power is supplied to minimize any possible noise ripple effects. At a minimum, place a 0.1uF and a 4.7uF capacitor on the UIM\_PWR supply and locate near the SIM connector.<sup>u</sup>



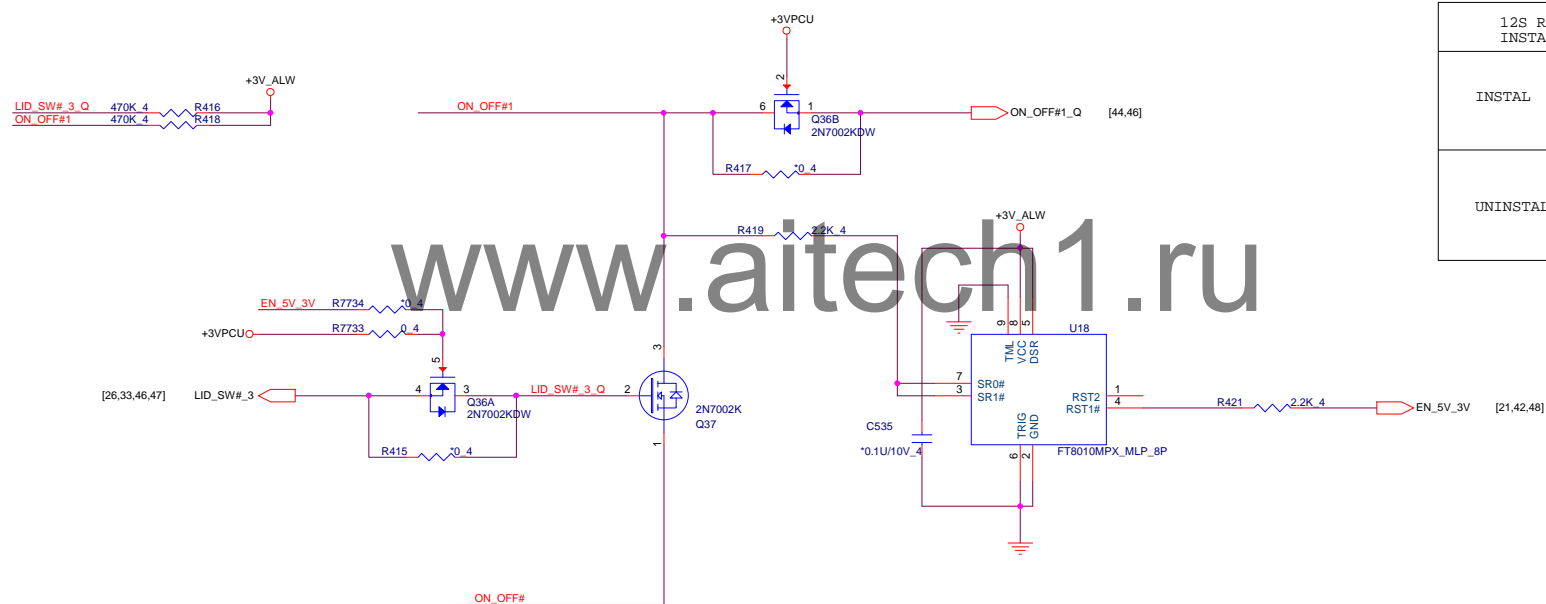
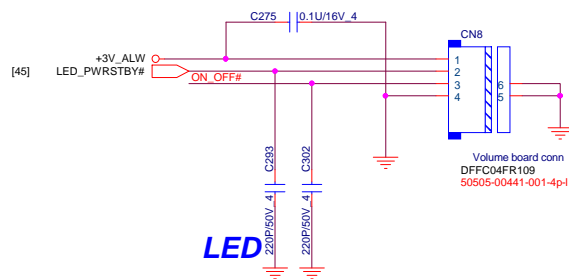
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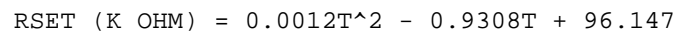


## Power Botton Connector



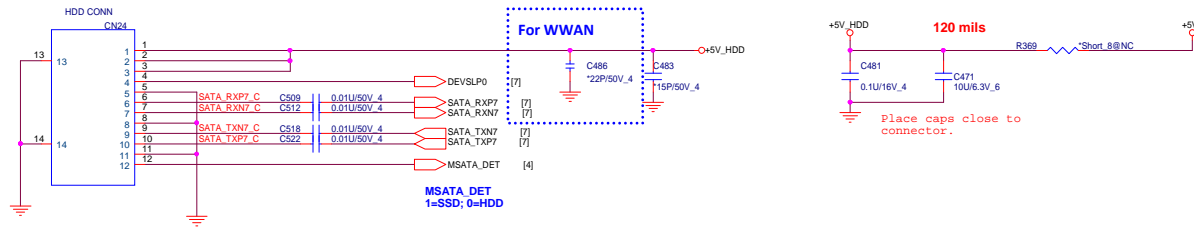
12S RESET MODE INSTAL FOR DB0		
INSTAL	R10702 R10704 R10701 U9068	R10703 R581 R595
UNINSTAL	R10754 Q7080	R10755 Q7081

[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63] +3V  
[8,27,29,30,40,42,43,54,58,63] +5V  
[9,48,51,52,58,62,63] +3V\_ALW

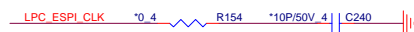
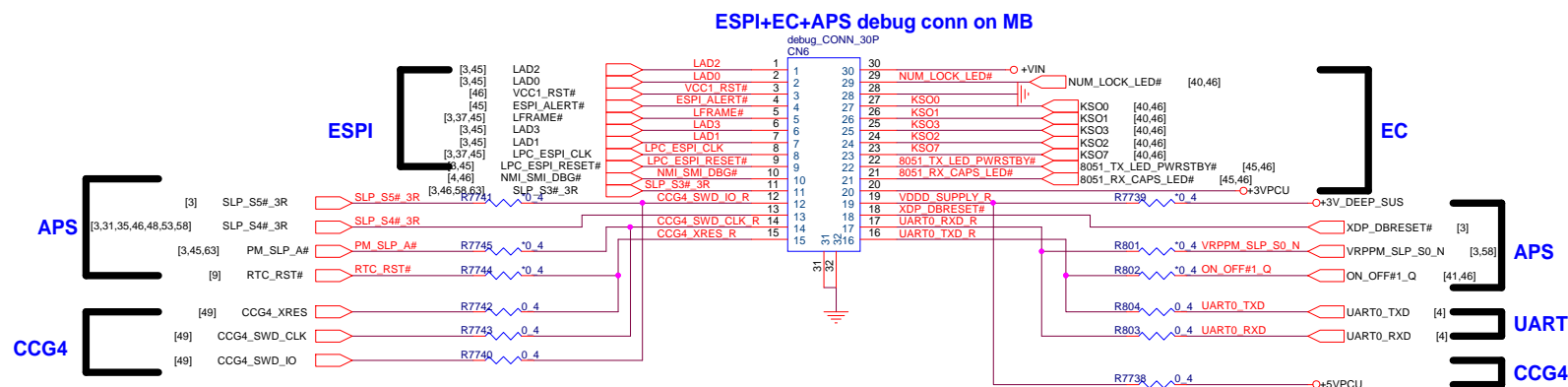


DEGREE	R476
70	36.5K
75	33.2K

# SATA-HDD



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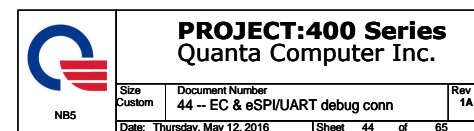


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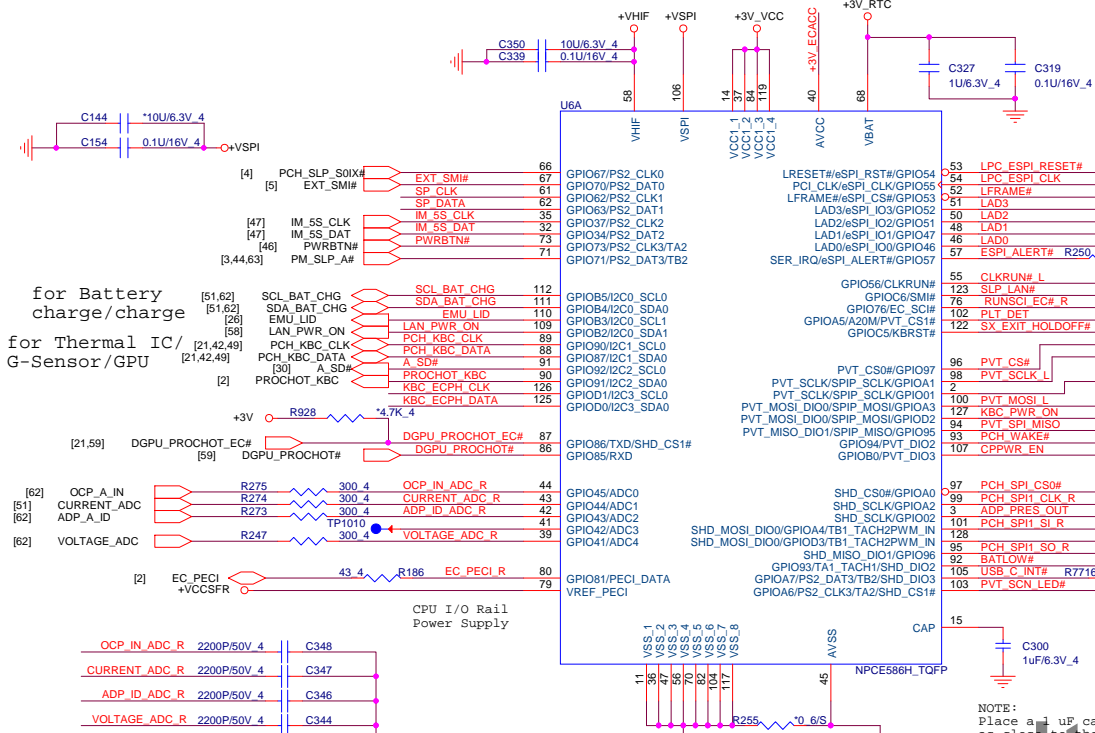


LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
R771	INSTAL	UNINSTAL
R769	UNINSTAL	INSTAL
R770	INSTAL	UNINSTAL

	LPC MODE	ESPI MODE
R658 <b>Ra</b>	INSTAL	UNINSTAL
R646 <b>Rb</b>	INSTAL	UNINSTAL
R659 <b>Rc</b>	INSTAL	UNINSTAL
R656 <b>Rd</b>	INSTAL	UNINSTAL
R649 <b>Re</b>	INSTAL	UNINSTAL
R657 <b>Rf</b>	INSTAL	UNINSTAL
R249 <b>Rg</b>	INSTAL	UNINSTAL
R147 <b>Rh</b>	INSTAL	UNINSTAL
R120 <b>Ri</b>	INSTAL	UNINSTAL
R276 <b>Rj</b>	INSTAL	UNINSTAL
R678 <b>Rk</b>	UNINSTAL	INSTAL

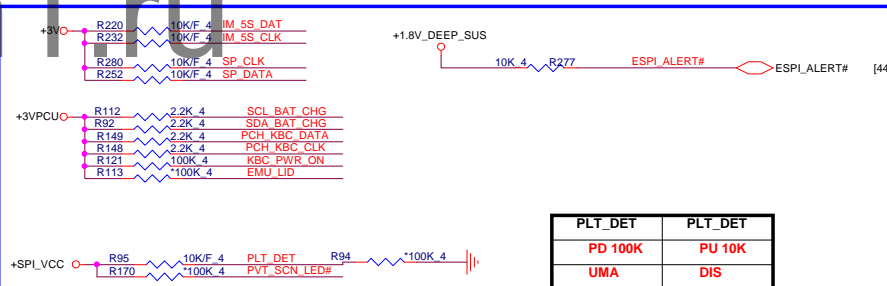
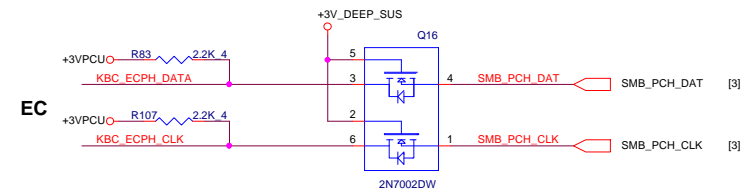
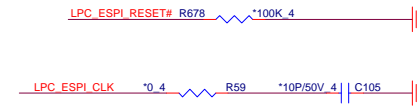




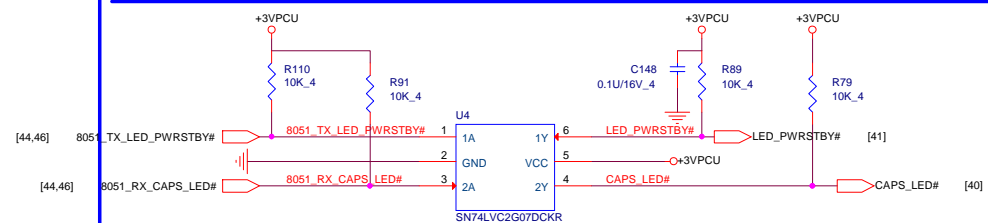


NOTE:  
Connect GND and AGND planes via an OR  
resistor or a one-point layout connection.

NOTE:  
Place a 1 uF capacitor  
as close to the CAP  
pin as possible.



PLT_DET	PLT_DET
PD 100K	PU 10K
UMA	DIS



8051\_TX\_LED\_PWRSTBY# R75 10K\_4 CAPS\_LED#  
8051\_RX\_CAPS\_LED# R102 10K\_4 LED\_PWRSTBY#

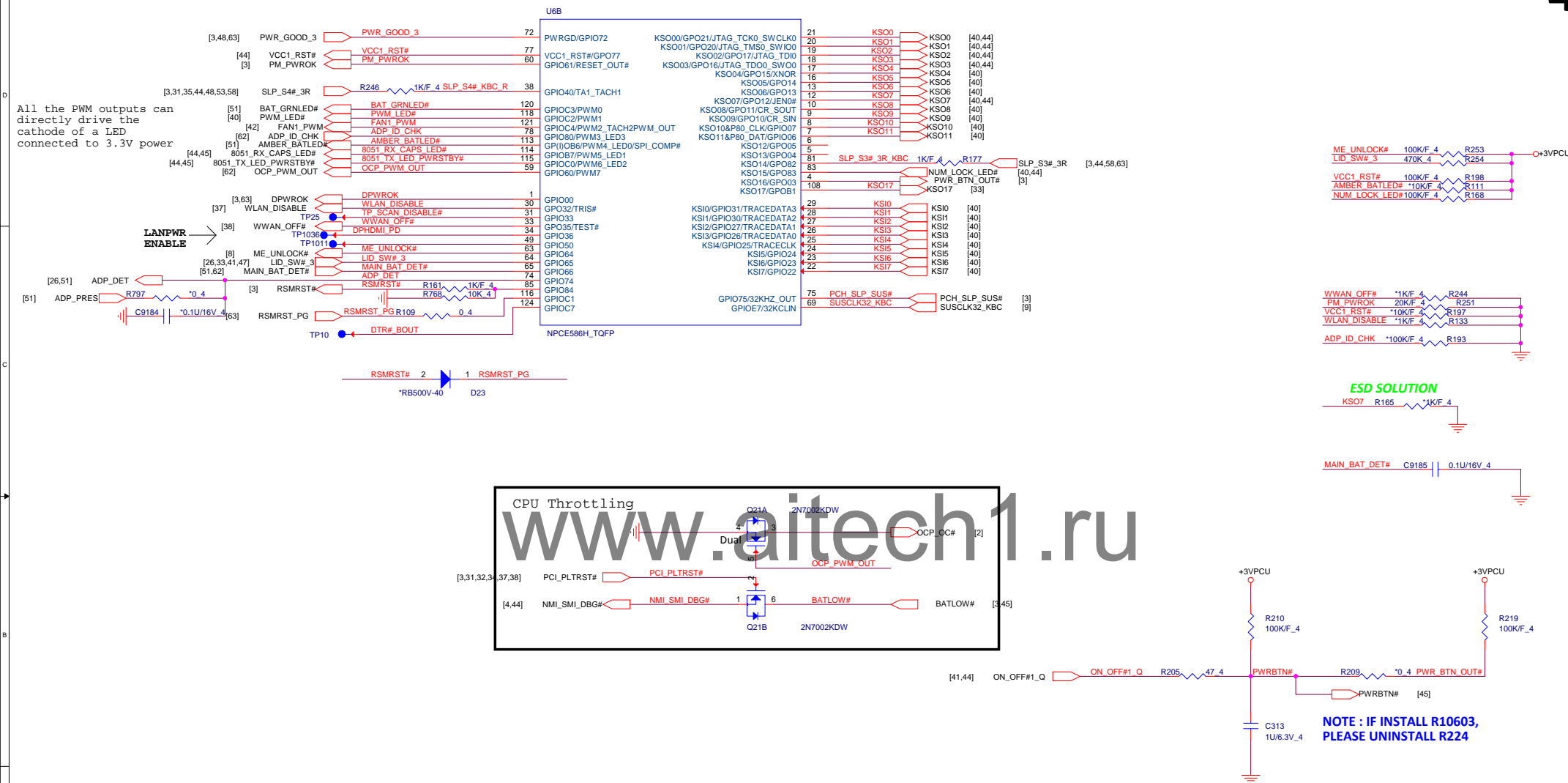


**PROJECT:400 Series**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	45 - EC NuvoTen NPCE586H_1	1A
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[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,47,51,56,58,59,63]  
[9,41,48,51,52,56,62,63]

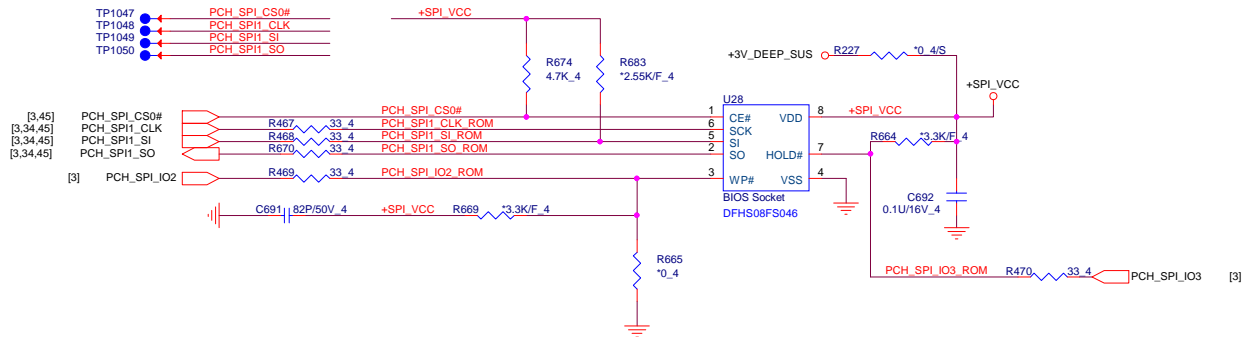
+3V  
+3V\_ALW



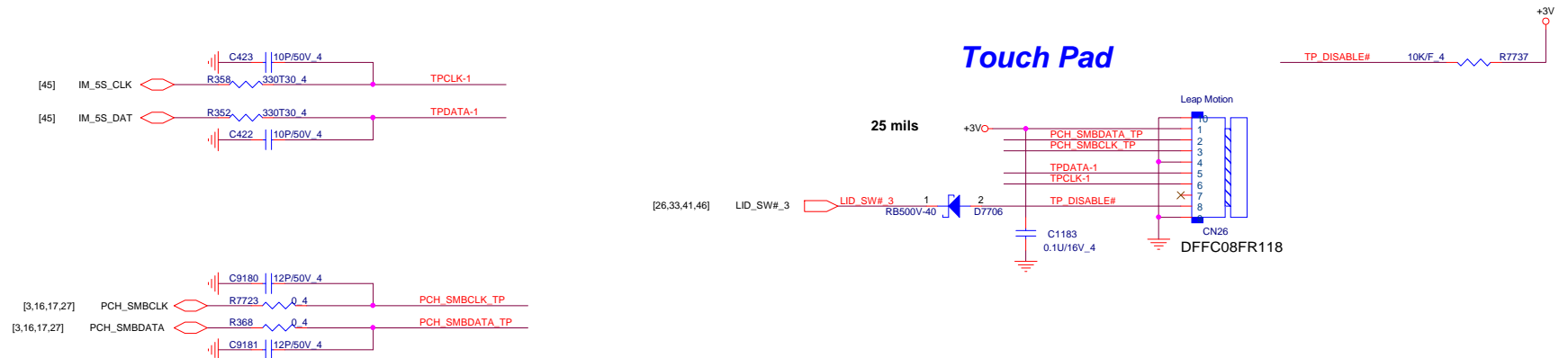
Vender	Size	P/N
GD	128MB	AKE2DF0KQ00
Winbond	128MB	AKE3DZKNK00
Socket		DFHS08FS046

## PCH SPI ROM(CLG)

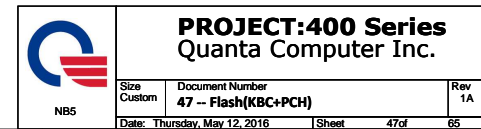
**PCH 6\*5mm WSON 16M  
SPI ROM Socket**



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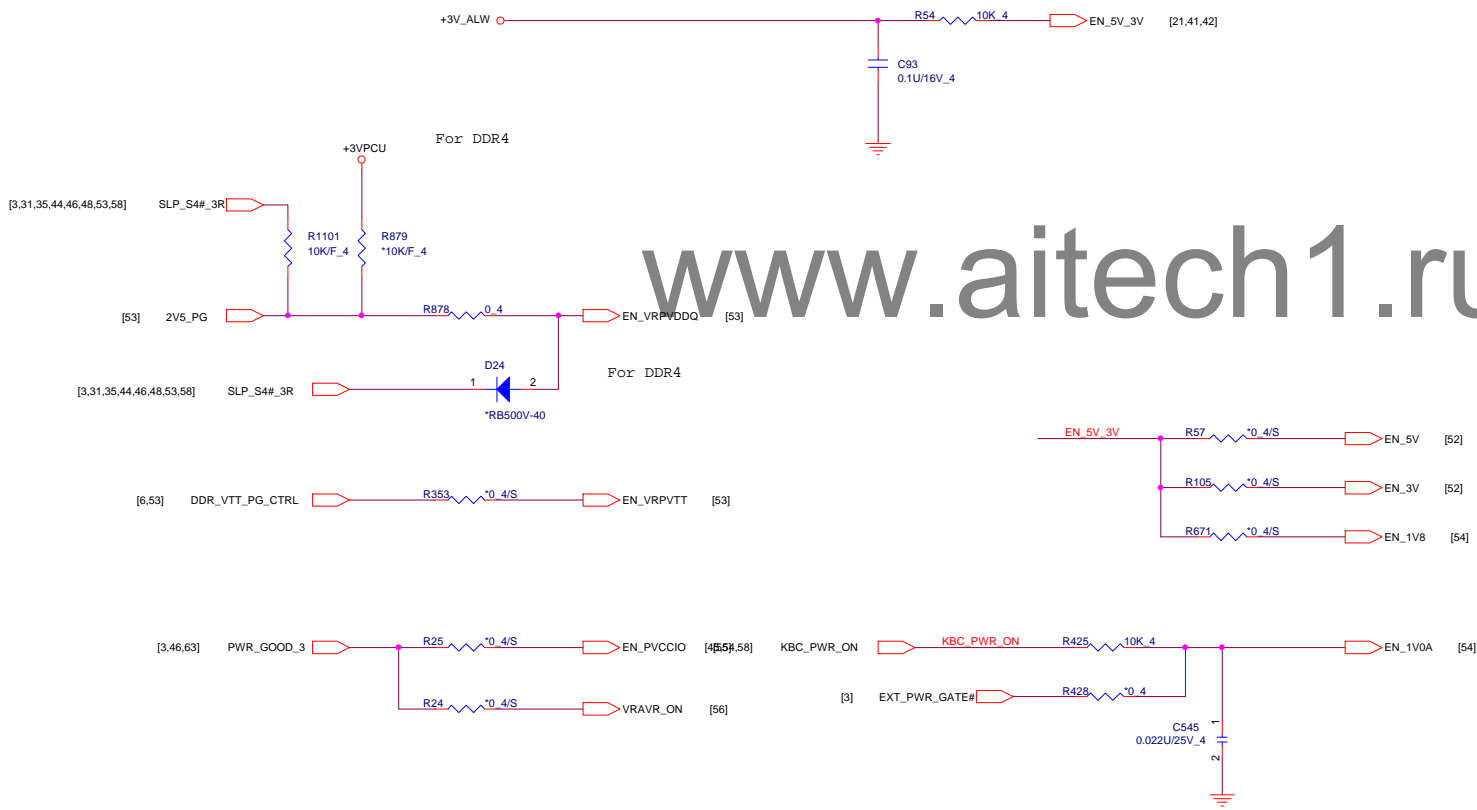


**CLICK PAD**  
Address: 0x20(7 bit)

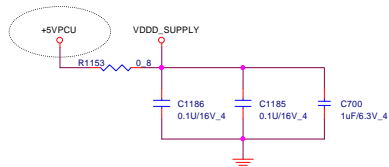


400 series 1001

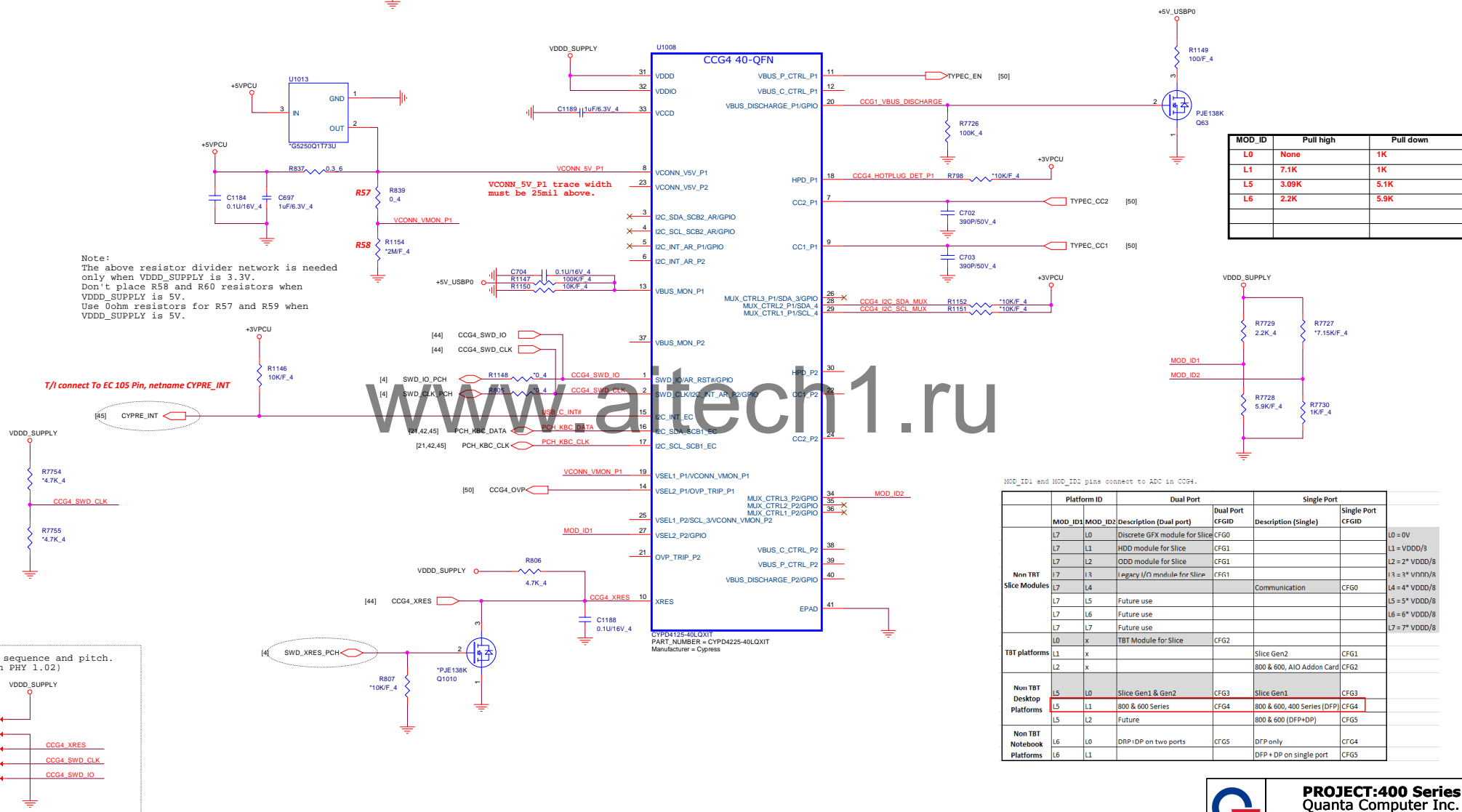
POWER TO EE NET NAME CONNECTION



**SI, 2/22, Change 5V**



Note:  
The above resistor divider network is needed only when VDD<sub>SUPPLY</sub> is 3.3V.  
Don't place R58 and R60 resistors when VDD<sub>SUPPLY</sub> is 5V.  
Use 0ohm resistors for R57 and R59 when VDD<sub>SUPPLY</sub> is 5V.

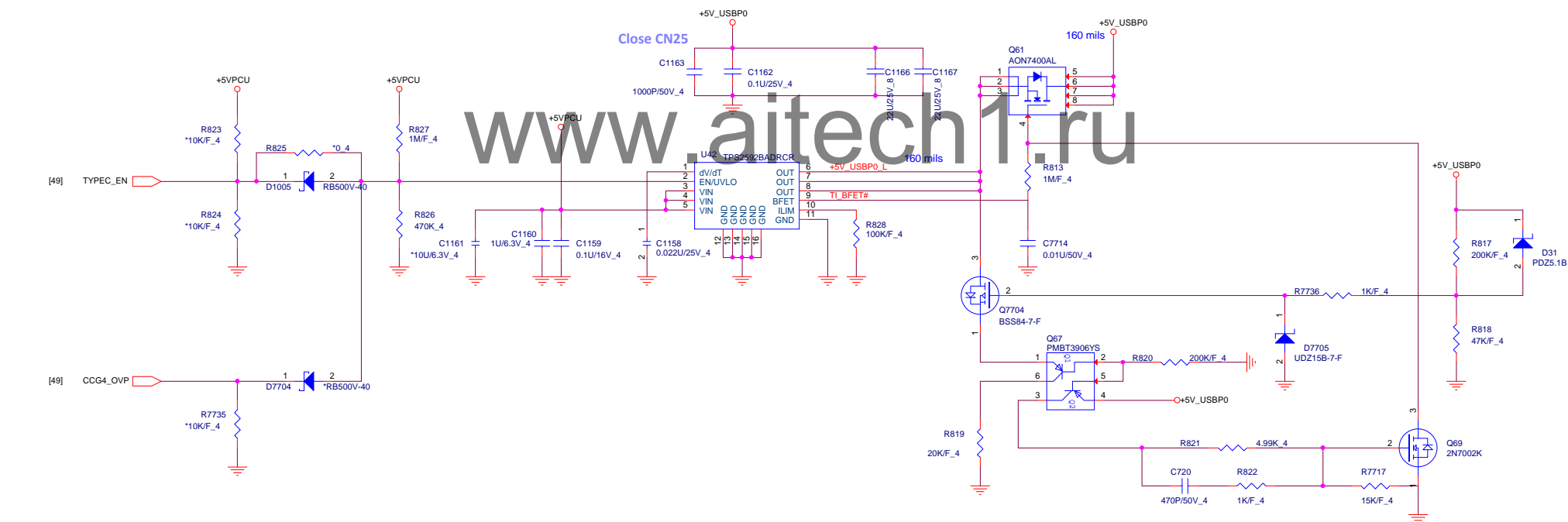


MOD_ID	Pull high	Pull down
L0	None	1K
L1	7.1K	1K
L5	3.09K	5.1K
L6	2.2K	5.9K

MOD ID1 and MOD ID2 pins connect to ADC in CCG4

	Platform ID		Dual Port	Single Port			
	MOD_ID1	MOD_ID2	Description (Dual port)	Dual Port CFGID	Description (Single)		Single Port CFGID
Non TBT Slice Modules	L7	L0	Discrete GFX module for Slice	CFG0			L0 = 0V
	L7	L1	HDD module for Slice	CFG1			L1 = VDD0/3
	L7	L2	ODD module for Slice	CFG1			L2 = 2* VDD0/3
	L7	L3	Legacy I/O module for Slice	CFG1			L3 = 3* VDD0/3
	L7	L4			Communication	CFG0	L4 = 4* VDD0/3
	L7	L5	Future use				L5 = 5* VDD0/3
	L7	L6	Future use				L6 = 6* VDD0/3
TBT platforms	L7	L7	Future use				L7 = 7* VDD0/3
	L0	x	TBT Module for Slice	CFG2			
	L1	x			Slice Gen2	CFG1	
Non TBT Desktop Platforms	L2	x			800 & 600, AIO Addon Card	CFG2	
	L5	L0	Slice Gen1 & Gen2	CFG3	Slice Gen1	CFG3	
	L5	L1	800 & 600 Series	CFG4	800 & 600, 400 Series (DPP)	CFG4	
	L5	L2	Future		800 & 600 (DPP+DP)	CFG5	
Non TBT Notebook Platforms	L6	L0	DRP iDP on two ports	CFG5	DPP only	CFG4	
	L6	L1			DPP + DP on single port	CFG5	



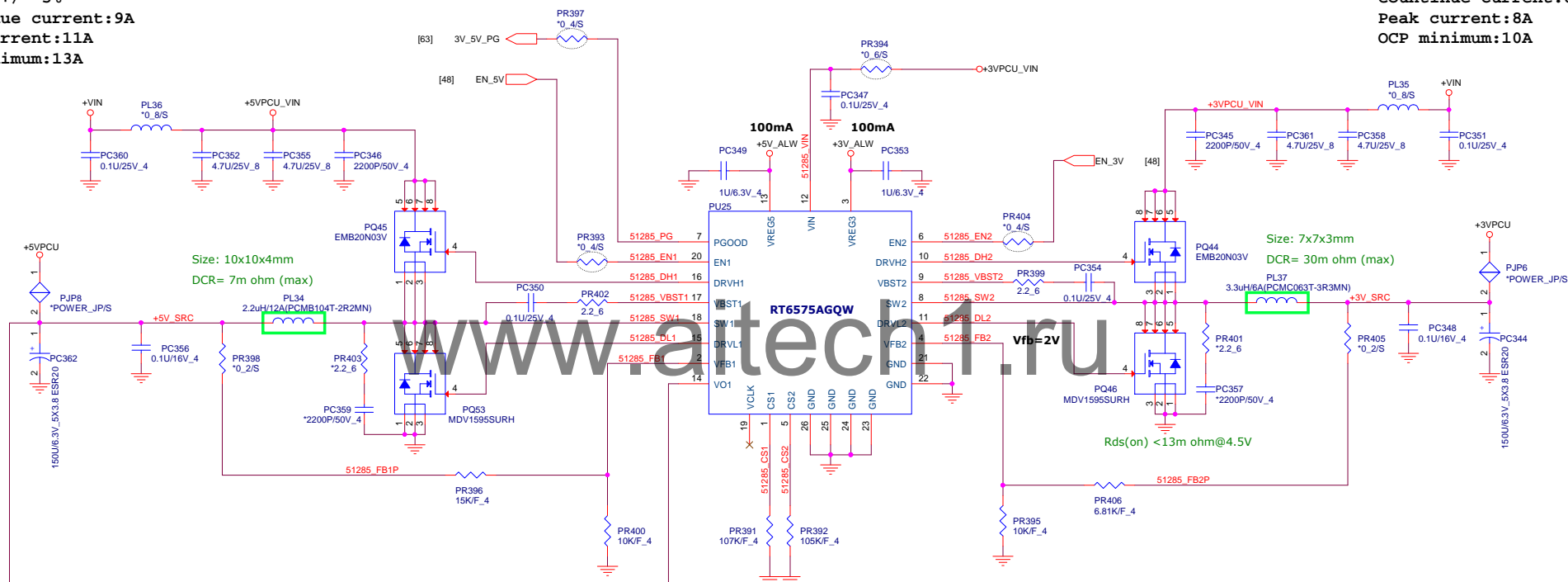




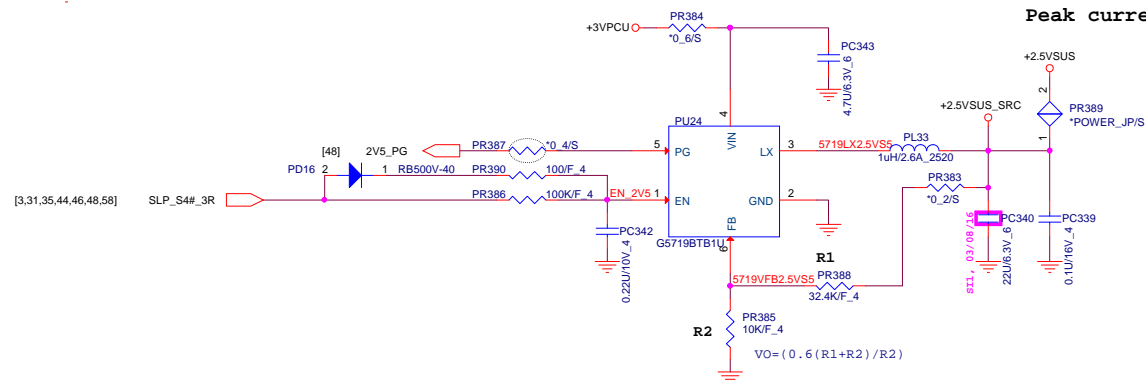
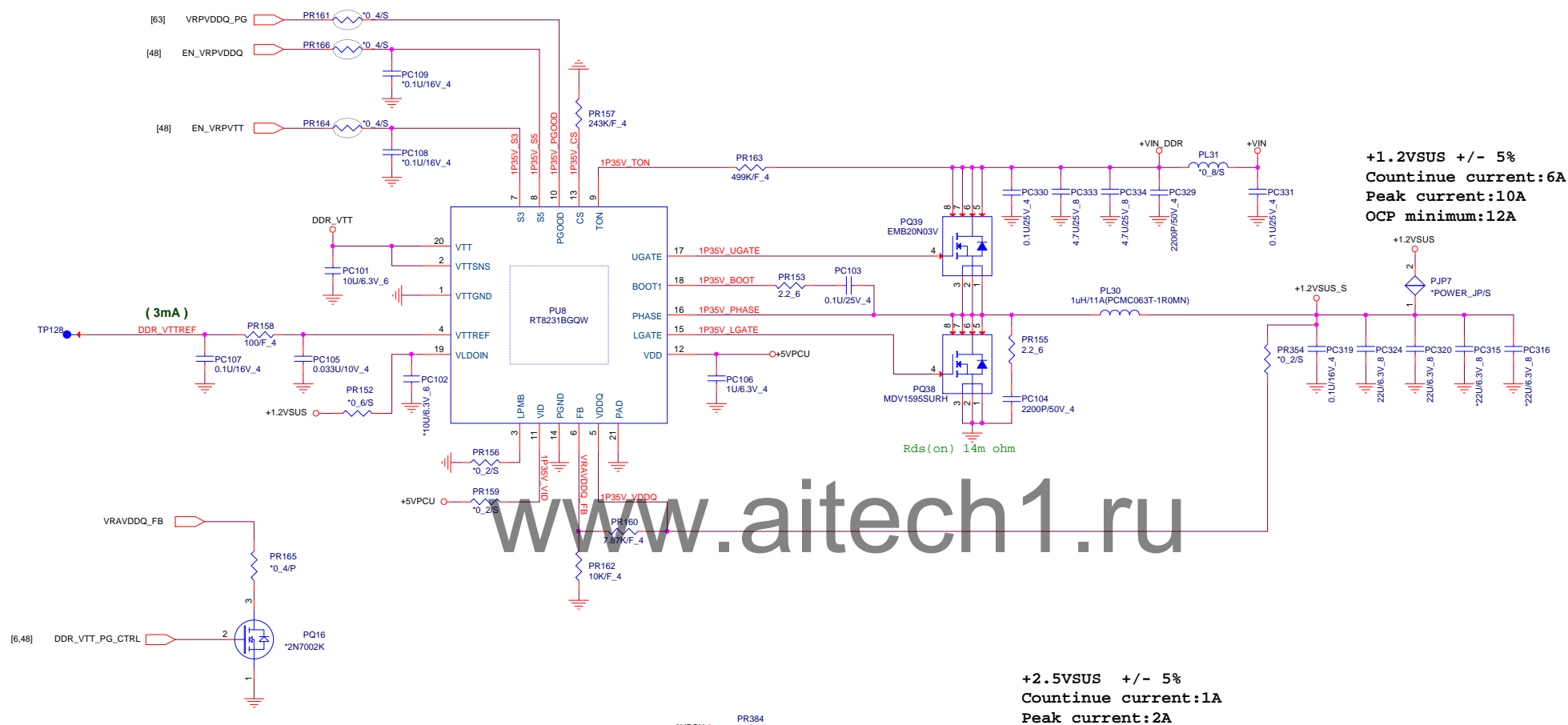
+3VPCU [3,10,33,37,38,40,41,42,44,45,46,48,49,51,53,55,58,60,62,63]  
+5VPCU [28,31,35,44,49,50,51,53,54,56,57,58,59,60,61,63]

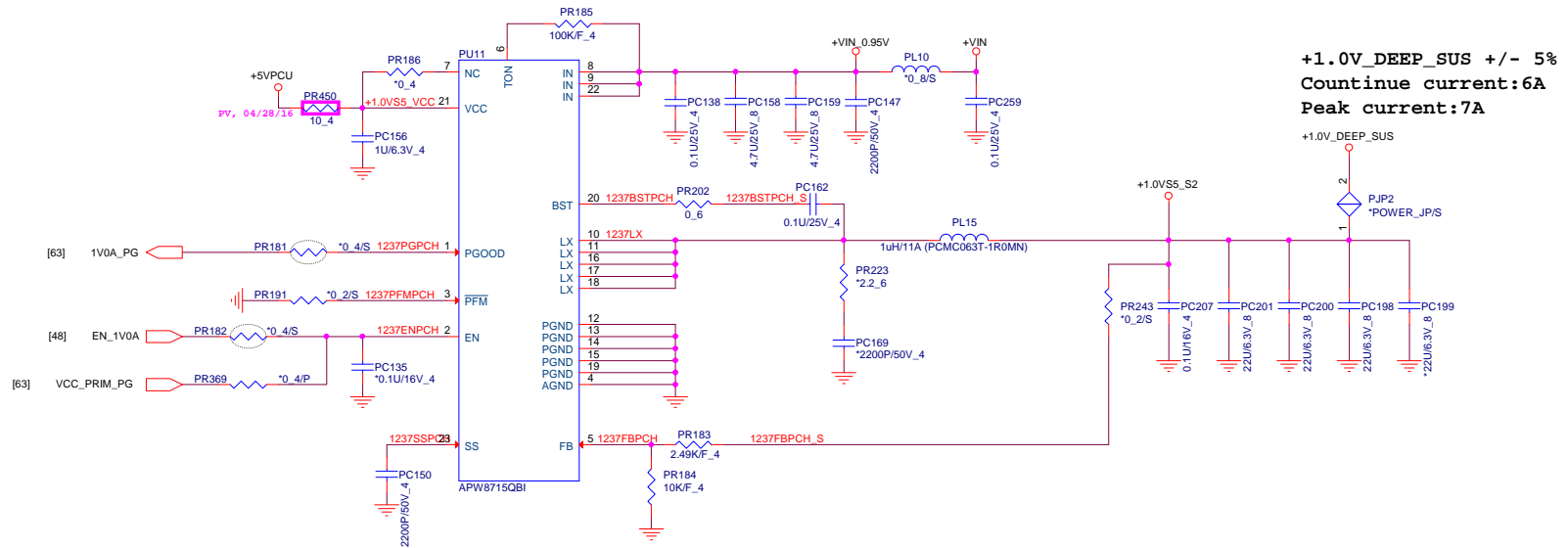
+5VPCU +/- 5%  
Continue current:9A  
Peak current:11A  
OCP minimum:13A

+3VPCU +/- 5%  
Continue current:6A  
Peak current:8A  
OCP minimum:10A



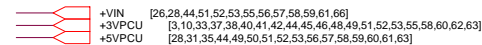
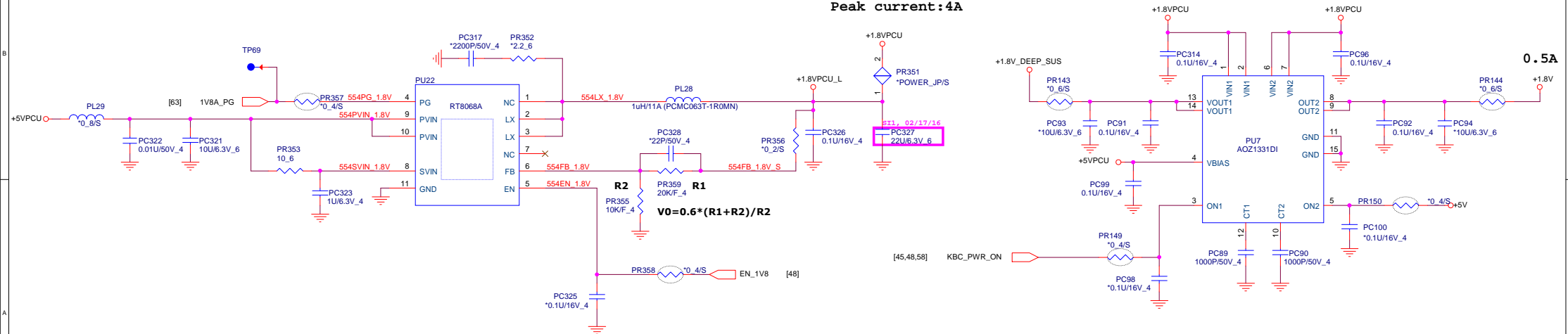






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+1.8VPCU +/- 5%  
Continue current:2A  
Peak current:4A

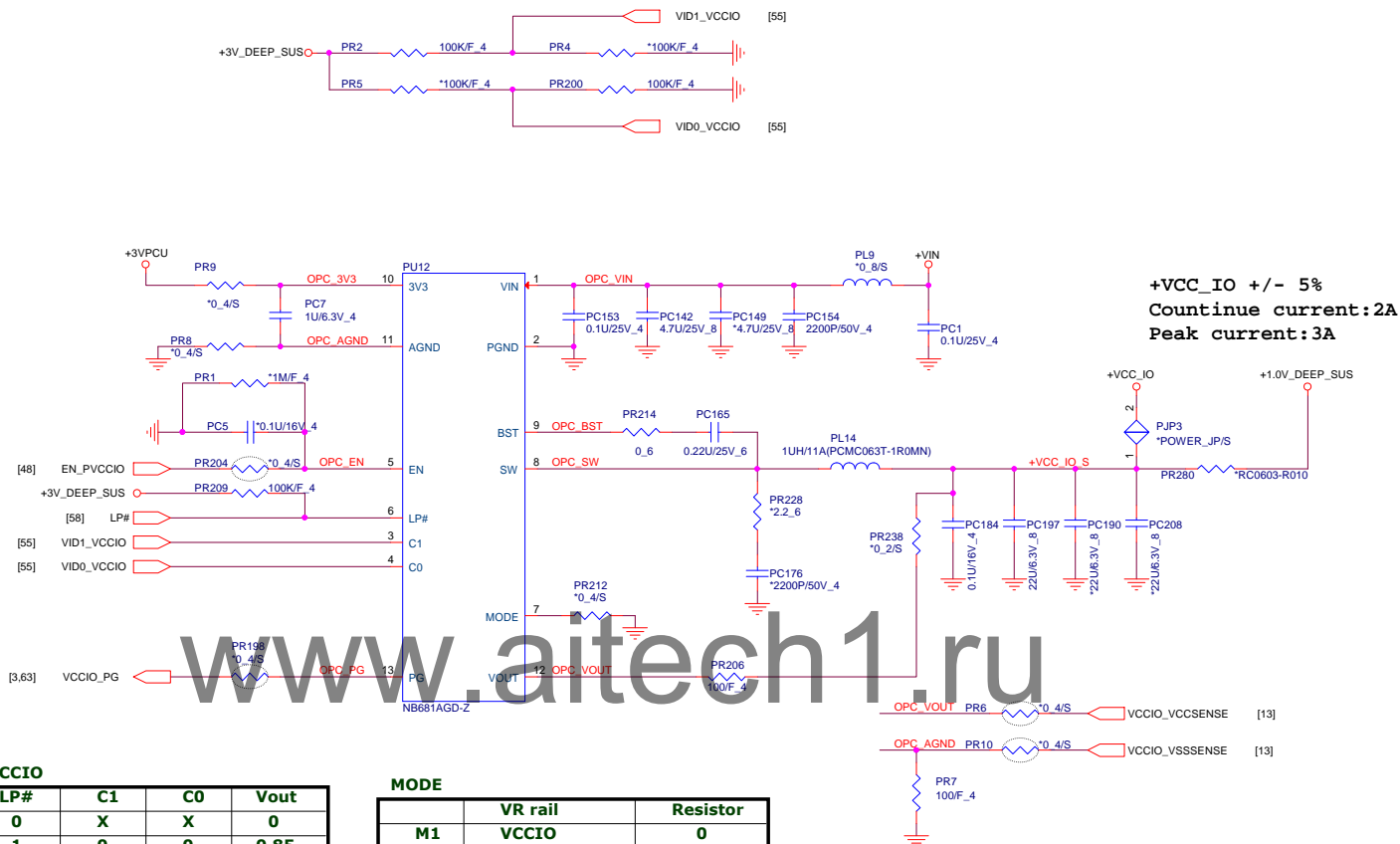


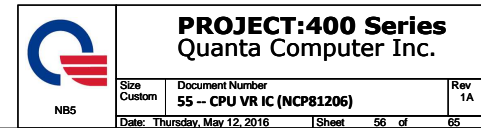
**PROJECT:400 Series**  
Quanta Computer Inc.

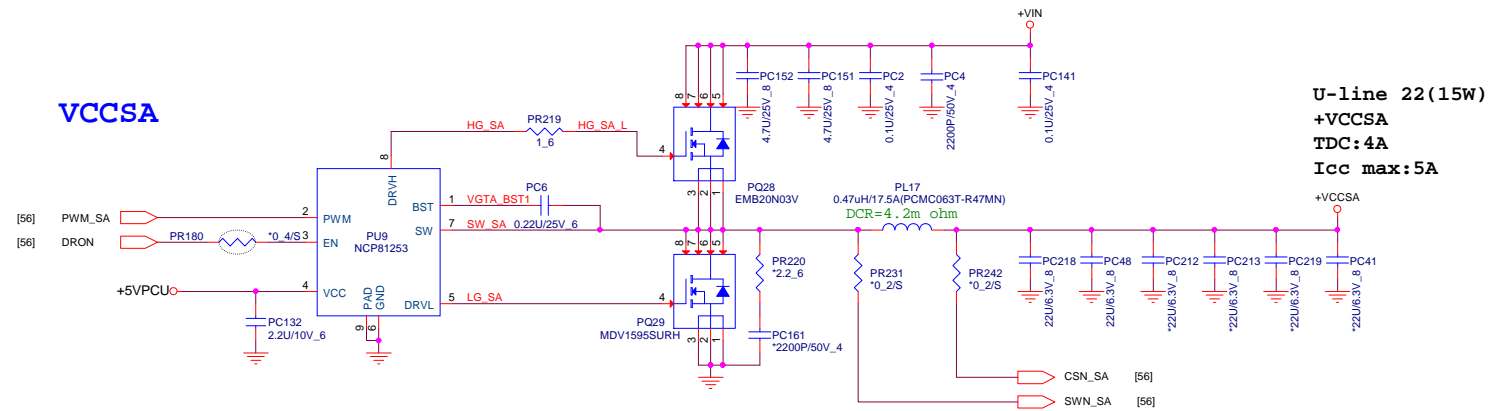
Size	Document Number 52 -- +1.0VS5/1.8VS5	Rev 1A
Date:	Thursday, May 12, 2016	Sheet 54 of 65

[26,28,44,51,52,53,54,56,57,58,59,61,66]  
[9,41,48,51,52,58,62,63]  
[5,13]

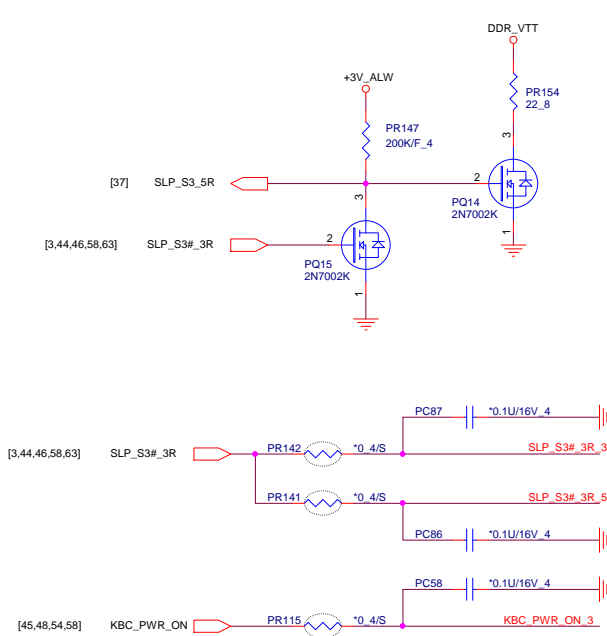
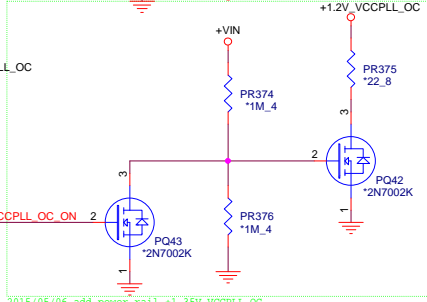
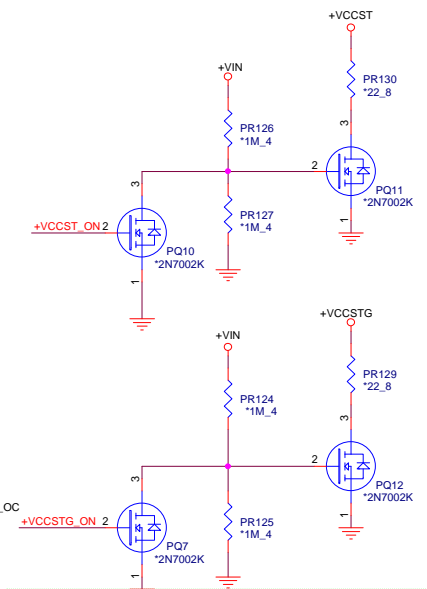
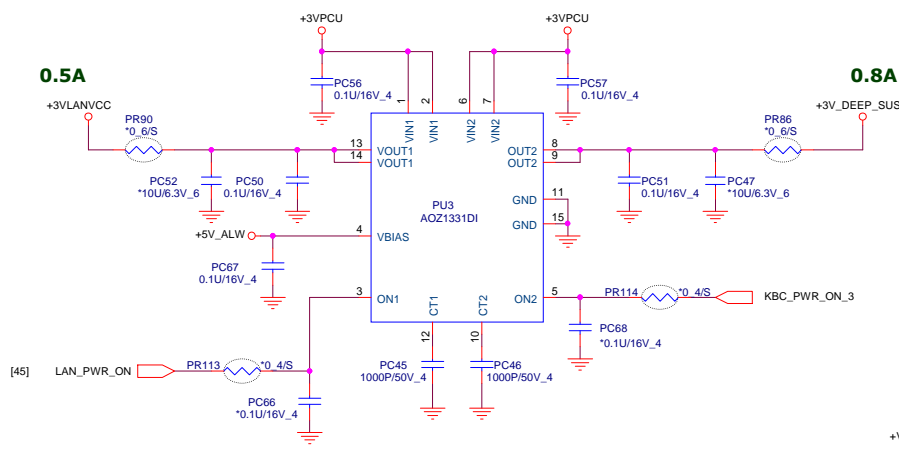
+VIN  
+3V\_ALW  
+VCC\_IO







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[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,59,63] +3V  
 [8,27,29,30,40,42,43,54,63] +5V  
 [28,29,44,51,52,63,54,55,56,57,59,61,66] +VIN  
 [3,10,33,37,38,40,41,42,44,45,46,48,49,51,52,53,55,60,62,63] +3VPCU  
 [28,31,35,44,49,50,51,52,53,54,56,57,59,60,61,63] +5VPCU  
 [32] +3VLAVCC



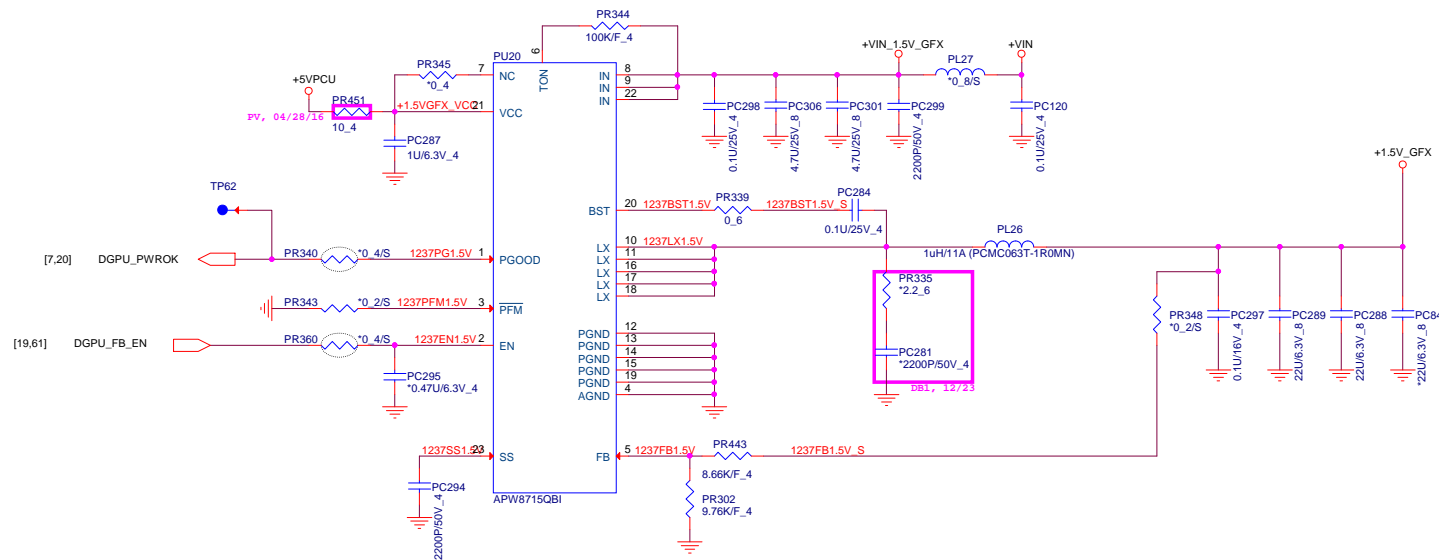
**PROJECT:400 Series**  
Quanta Computer Inc.

Size Custom	Document Number <b>57 -- Load switch IC (APL3523A)</b>	Rev 1A
Date: Thursday, May 12, 2016	Sheet	58 of 65



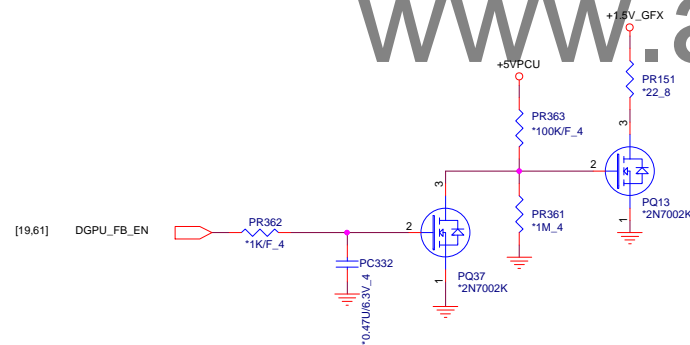






**+1.5V\_GFX Volt +/- 5%**  
**Countinue current:2.4A**  
**Peak current:4.1A**  
**OCP minimum:8A**

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# POK CKT

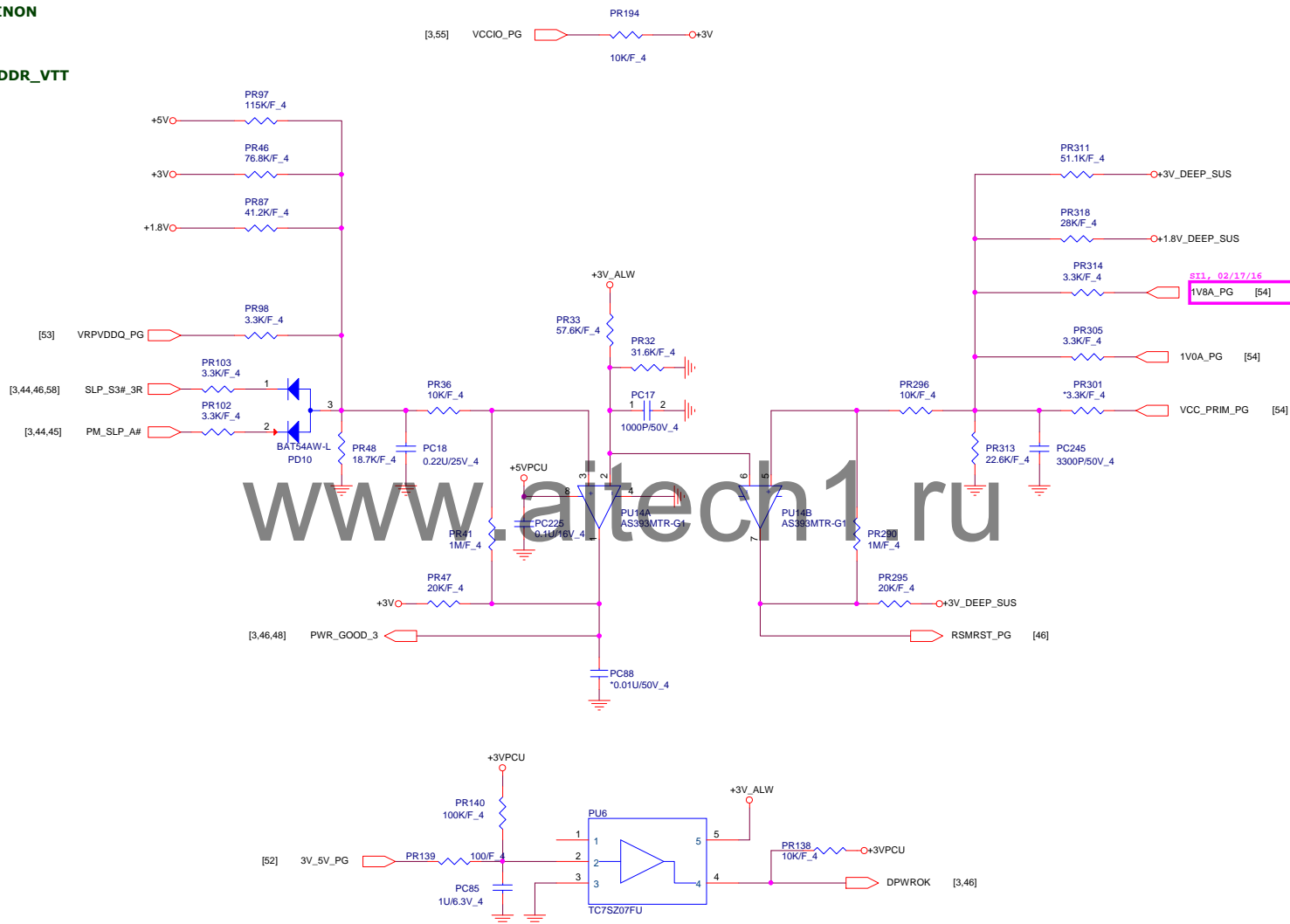
PM\_SLP\_S4# = SUSON

PM\_SLP\_S3# = MAINON

+V5S = +5V

+V3S = +3V

+V0.75S = +0.75V\_DDR\_VTT




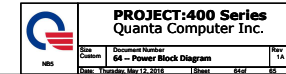
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[8,27,29,30,40,42,43,54,58]

[9,41,48,51,52,58,62]

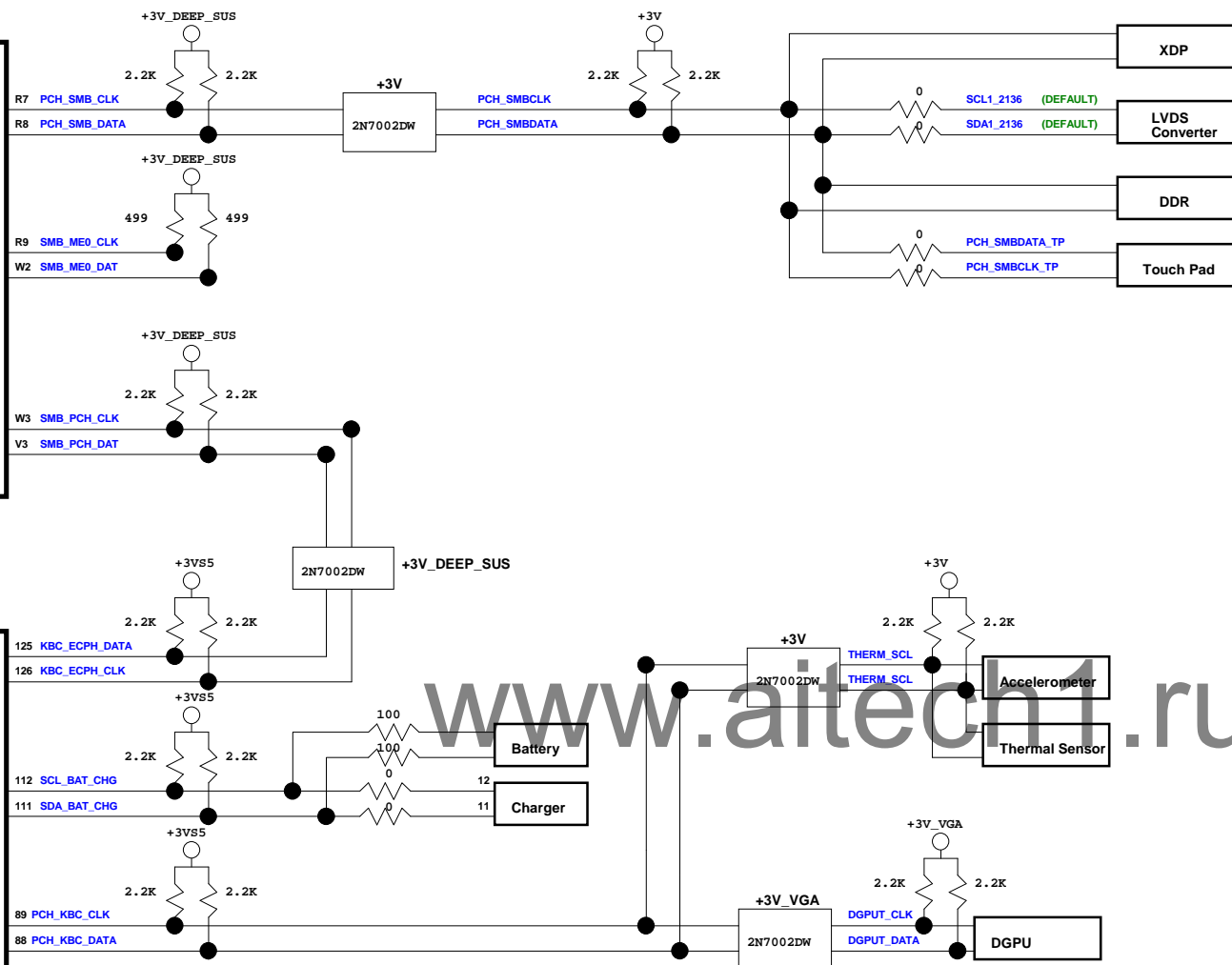
+3V  
+5V  
+3V\_ALW

	<b>PROJECT:400 Series</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>63 - PWROK</b>	Rev 1A
	Date: Thursday, May 12, 2016	Sheet 63 of 65	



SKYLAKE U

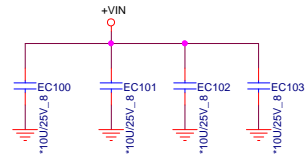
EC  
NPCE586H



Example: \*499/F\_4 and \*0\_6/S  
 \* means none-installed  
 499 means value  
 F means 1%  
 \_4 means 0402 size  
 /S means short pad

Multiplexed HSIO Lane	Port Assignment
USB3 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB3 #2 / SSIC #1	USB2.0/USB3.0 Combo Jack(Left side up)
USB3 #3 / SSIC #2	NC
USB3 #4	NC
PCIE1 / USB3 #5	dGPU
PCIE2 / USB3 #6	dGPU
PCIE3	dGPU
PCIE4	dGPU
PCIE5	LAN
PCIE6	WLAN
PCIE7 / SATA #0	HDD (SATA)
PCIE8 / SATA #1	ODD (SATA)
PCIE9	Cardreader (PCIE)
PCIE10	NC
PCIE11 / SATA #1*	NC
PCIE12 / SATA #2	SSD (SATA)

USB2.0	Port Assignment
USB2 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB2 #2	USB2.0/USB3.0 Combo Jack(Left side up)
USB2 #3	WWAN
USB2 #4	USB2.0(Right side on USB Board)
USB2 #5	USB2.0(Right side on USB Board)
USB2 #6	Touch Screen
USB2 #7	Bluetooth
USB2 #8	Finger Print
USB2 #9	Camera
USB2 #10	NC



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